

# COMPAL CONFIDENTIAL

MODEL NAME :  
FDI40 N3-14", FDI4A V3-14", FDI43 N5-14",  
FDI50 N3-15", FDI5A V3-15", FDI53 N5-15",  
FDI70 N3-17"

PCB NO : DA8001K6000 (SBDR)  
DA8001K6100 (NBDR)

BOM P/N :  
SBDR-DIS NBDR-DIS X4E  
431AJ431L51 431AJ431L01 X4E AJ431L51(N3)  
431AJ431L52 431AJ431L02 X4E AJ431L52(V3)  
431AJ431L53 X4E AJ431L01(N5)  
431AJ431L54

## CML-U+MEC1418

### 2019-06-20

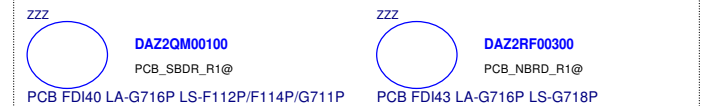
REV : 1.0 (A00)

@ : Un-pop Component  
DIS@ : GPU Support  
INSPIRON@/VOSTRO@ : Inspiron/Vostro  
CML@/CNL@ : CML/CNL  
BASE@/PREM@ : Pentium,Celeron / i3,i5,i7  
EXO@/TOPAZ@ : R17M-M1-30/R17M-M2-50  
EC@ : EC Support  
JP@/PJP@ : JUMP  
100@/1000@: Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
KBBL@ : KB Backlight  
TPM@/FTPM@ : HW TPM/SW TPM  
750\_CTPM@:750 and china TPM  
ST\_CTPM@:ST and china TPM  
CTPM@:China TPM  
FFS@ : Free Fall Sensor  
TYPEC@ : TypeC  
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component  
M1\_30@/M2\_50@ : R17M-M1-30/R17M-M2-50  
2G\_G5@/2G\_H@/2G\_S@/2G\_M@ : VRAM type  
PCB@/PCB\_R1@/PCB\_R3\_G@/PCB\_R3\_T@/PCB\_R3\_H@/PCB\_R3\_TM@: PCB MB

PCB\_NBDR\_R1@: PCB MB DAZ for NBDR  
TS\_NON@/TS\_USB@/TS\_I2C@: Touch Screen Interface Select  
SBDR@/NBDR@: SBDR/ NBDR Select

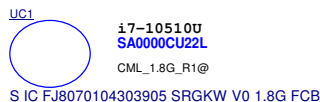
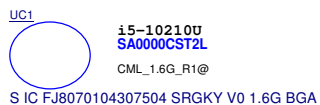
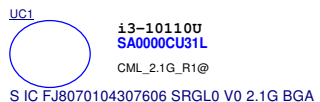
### PCB R1



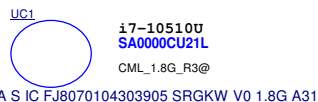
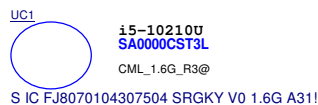
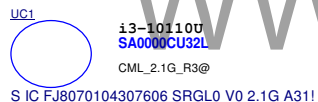
### PCB R3



### CPU R1



### CPU R3



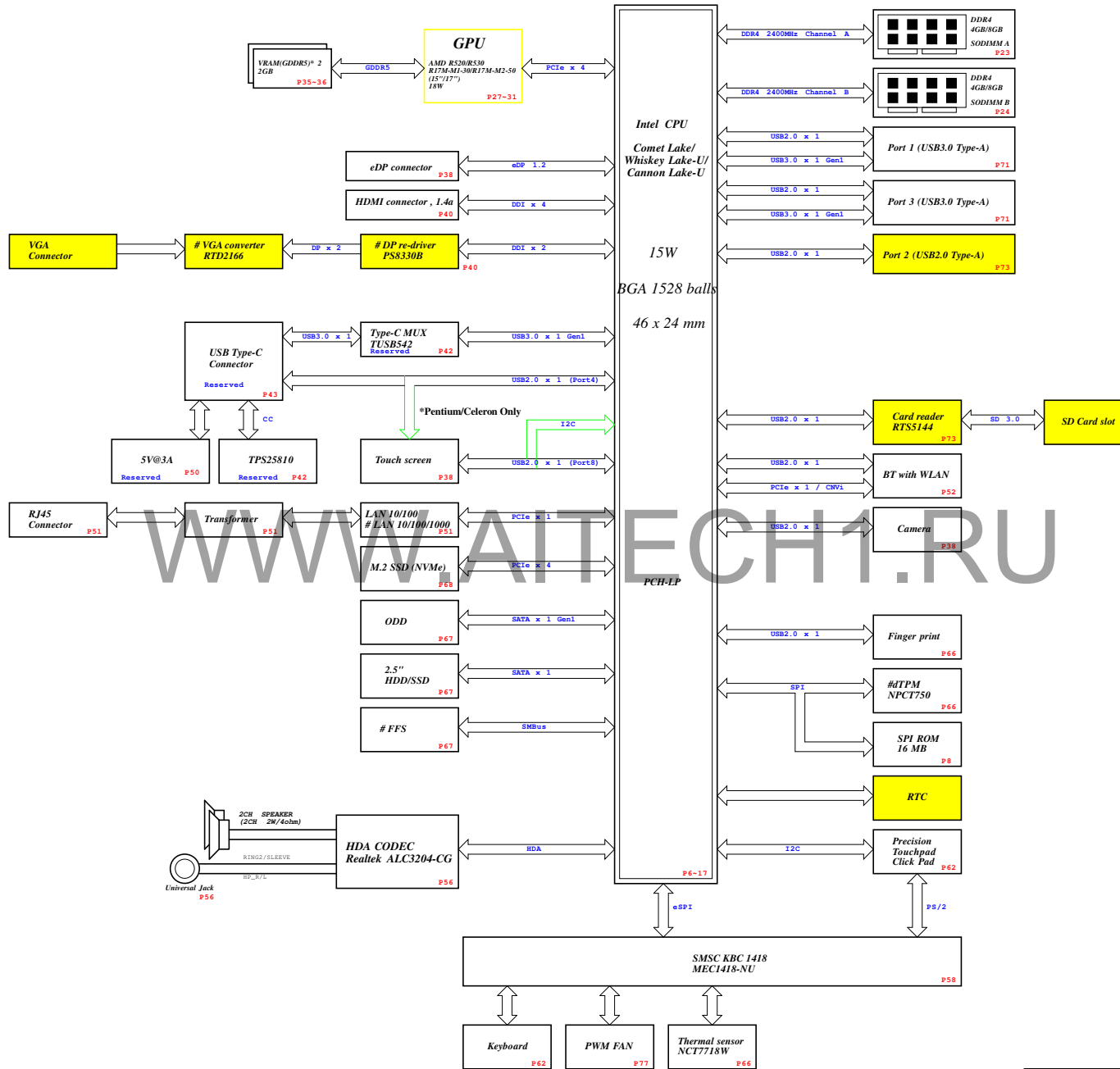
Layout Dell logo



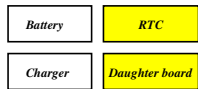
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REV: X01  
PWB: 9HTP8



















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Size	Document	Number	Rev	LA-G716P	
Date:	Thursday, June 20, 2019	Sheet	1 of 101	Rev 1.0	

## Block Diagram



# ----> V3 only



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 Port, IO/B
4*	Touch screen
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Reserved
9	NA
10	BT

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100	10.0	3.000	EVT	SBDR-UMA
2	100	17.8	2.801	DVT1	
3	100	27.0	2.598		NBDR-UMA
4	100	37.4	2.402	DVT2	
5	100	49.9	2.201		SBDR-DSC
6	100	64.9	2.001	Pilot	
7	100	82.5	1.808		NBDR-DSC
8	100	107.0	1.594		
9	100	154.0	1.299		
10	100	200.0	1.100		

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes

USB3.0	PCIe	SATA	DESTINATION
USB3.0-1	PCIe-1		USB3.0 port1
USB3.0-2	PCIe-2		NA
USB3.0-3	PCIe-3		USB3.0 port2
USB3.0-4	PCIe-4		TypeC
USB3.0-5	PCIe-5		GPU
USB3.0-6	PCIe-6		GPU
	PCIe-7		GPU
	PCIe-8		GPU
	PCIe-9		LOM
	PCIe-10		WLAN
	PCIe-11	SATA-0	SATA HDD
	PCIe-12	SATA-1A	SATA ODD
	PCIe-13		NVME SSD
	PCIe-14		NVME SSD
	PCIe-15	SATA-1B	NVME SSD
	PCIe-16	SATA-2	NVME SSD

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LA-G716P				Rev
Title: Thermal Area 2019				Rev: 1 of 101

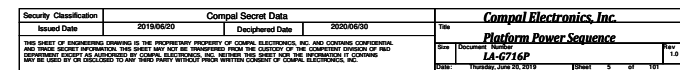
DELL CONFIDENTIAL/PROPRIETARY

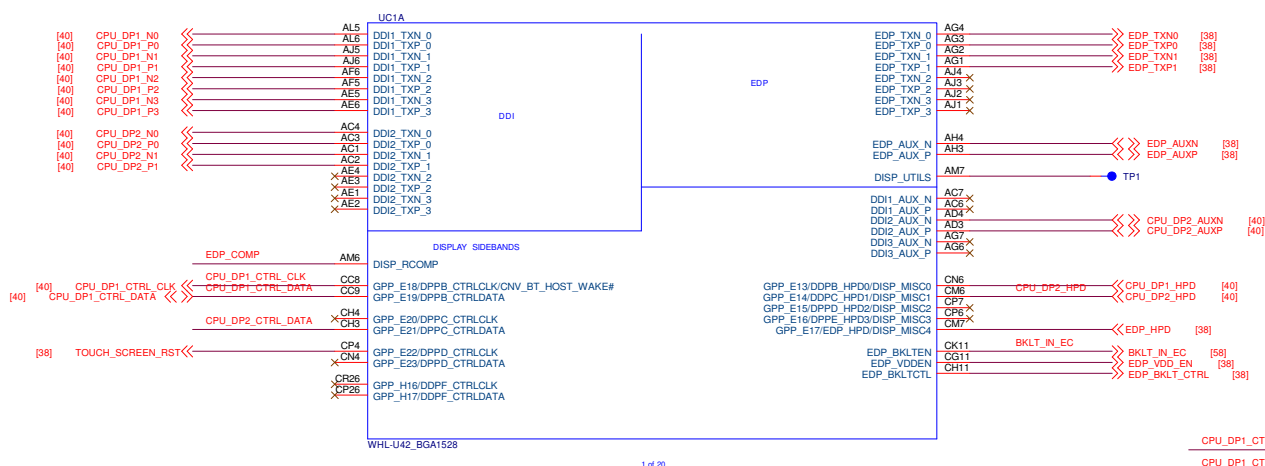
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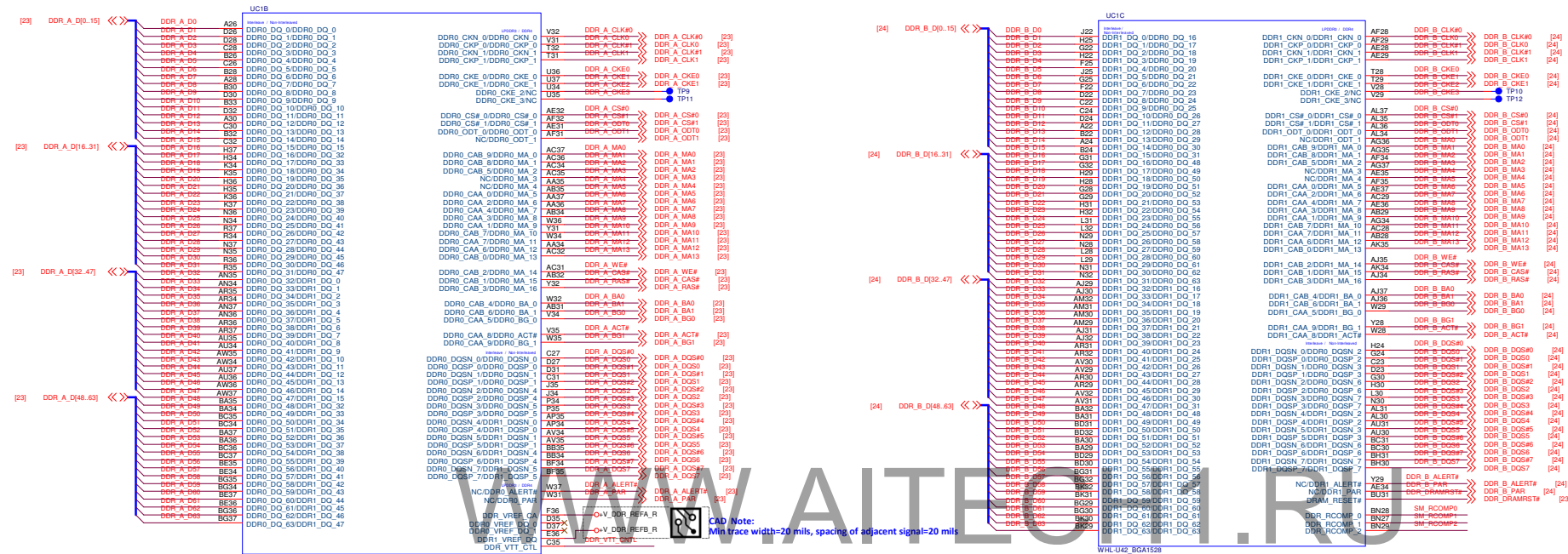
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Date:				Thursday, June 20, 2019	Sheet	6 of 101

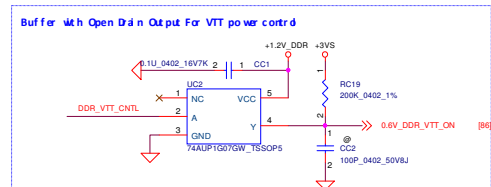
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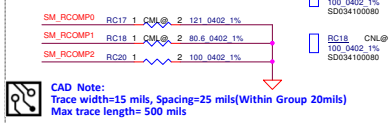
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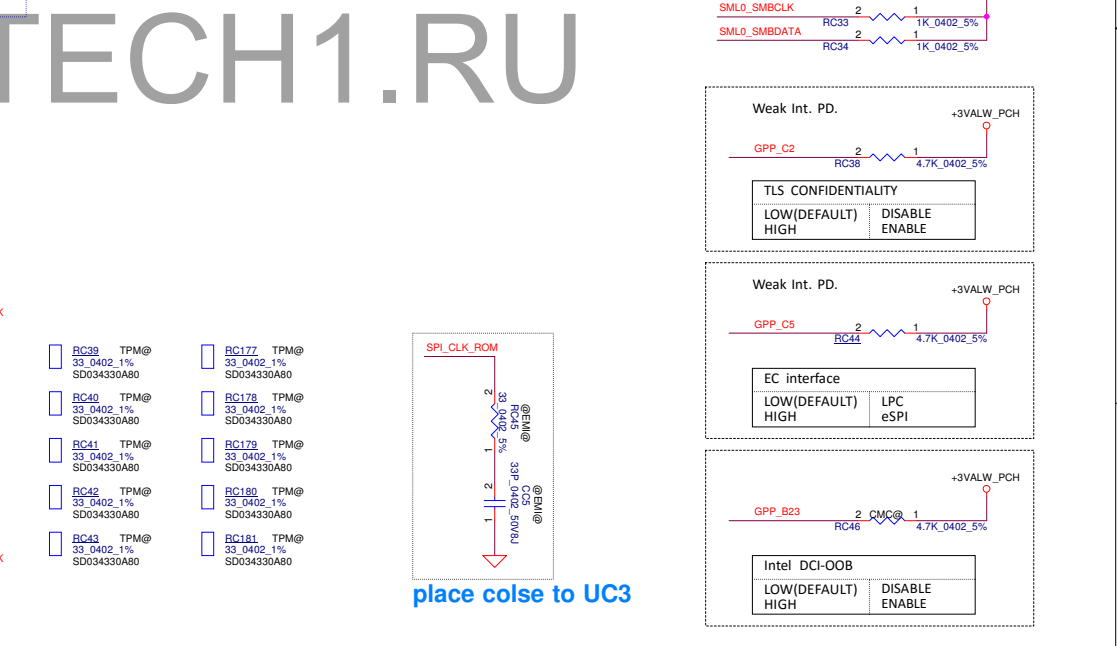
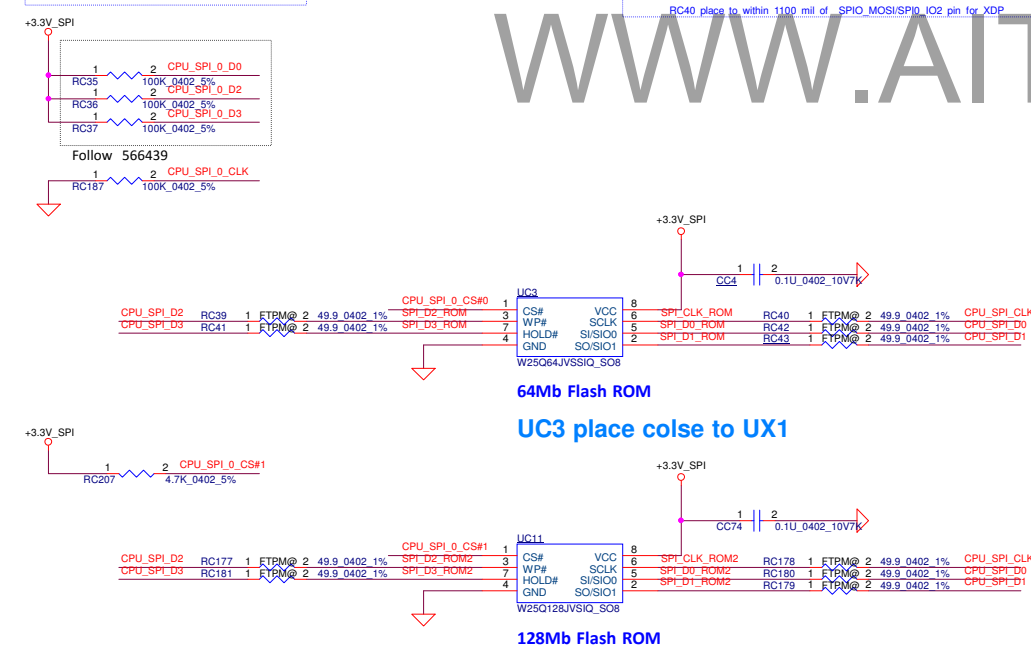
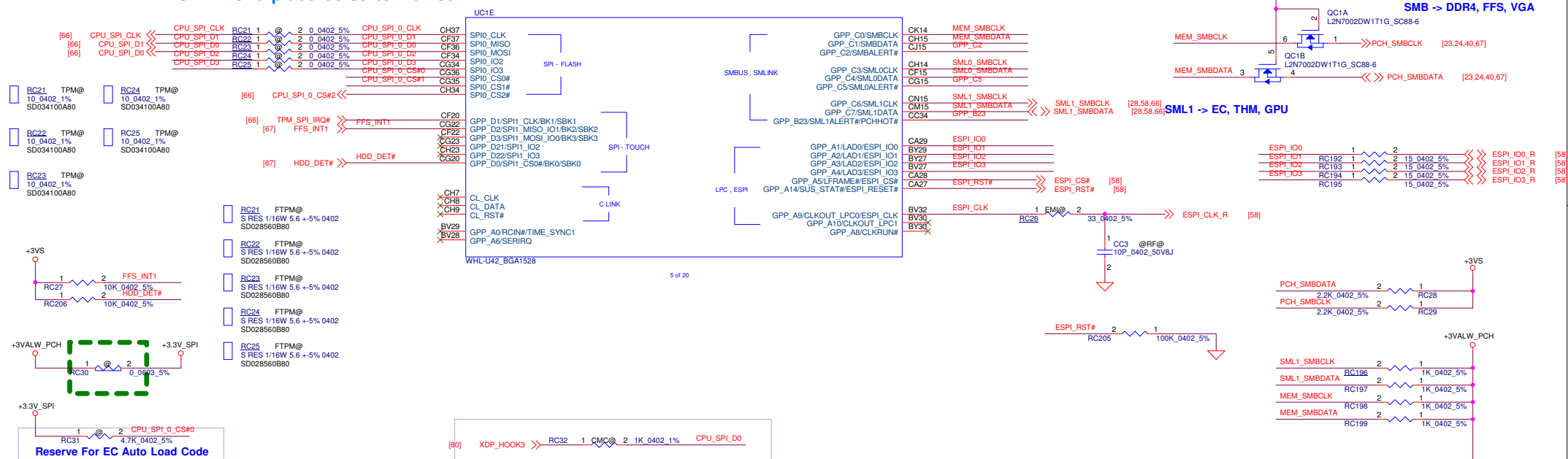
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## DDR4 COMPENSATION SIGNALS

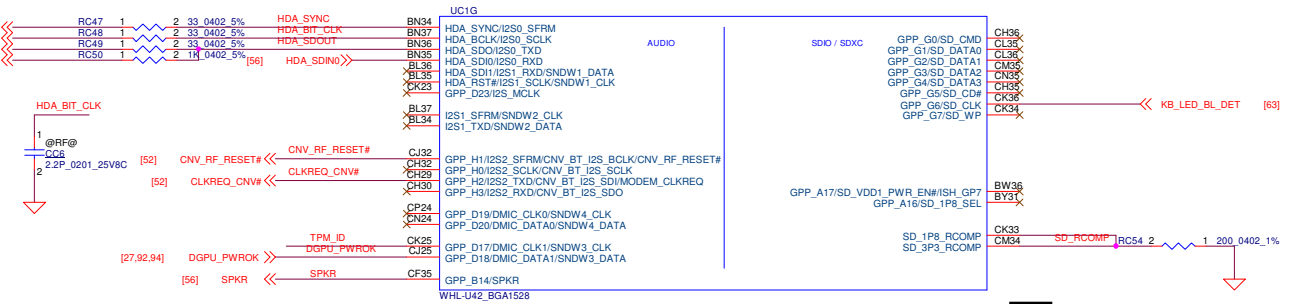
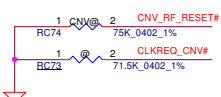
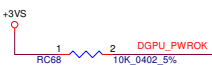
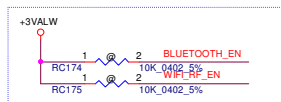
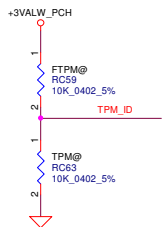
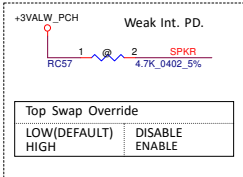
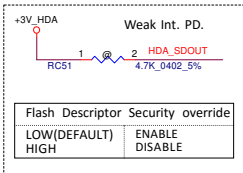


**RC21~RC25 place colse to Device**



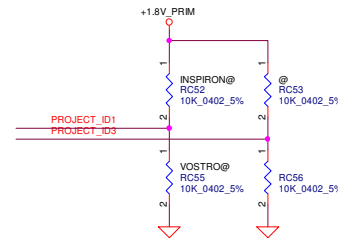
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				Size Custom	Document Number	Rev
				LA-G716P 1.0		
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ME\_FWP  
LOW = ENABLE -->ME lock, can't update ME  
HIGH = DISABLE -->ME un-lock, can update ME

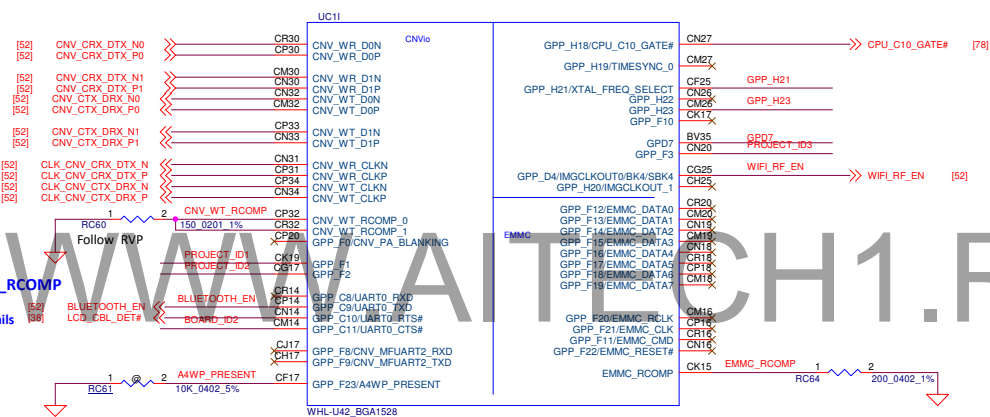


COMPENSATION FOR SD\_ROMP

CAD Note:  
Min trace width=10 mils, Spacing=12 mils  
Max trace length=500 mils

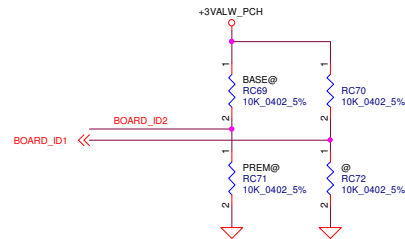
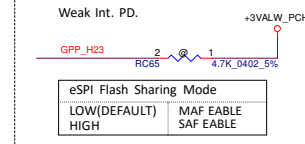
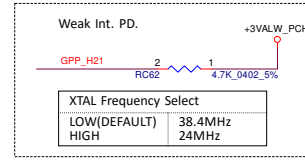


RC53,RC56	eMMC SKU Opt i on d
LOW	Standard
HIGH	Narrow Border

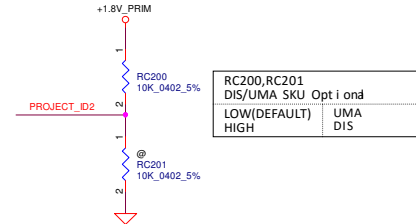


COMPENSATION FOR EMMC\_ROMP

CAD Note:  
Min trace width=10 mils, Spacing=12 mils  
Max trace length=500 mils



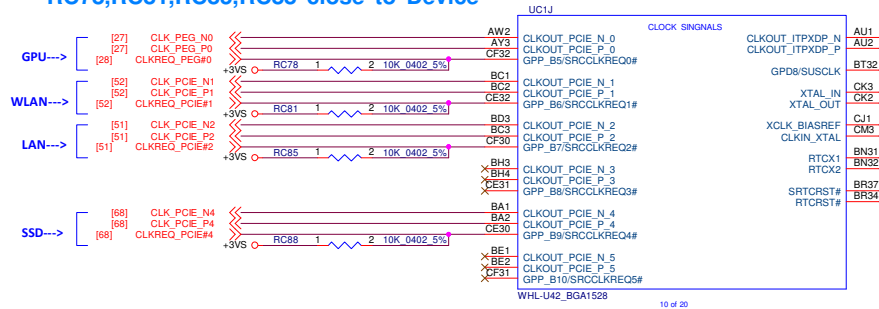
CPU ID	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
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WHL-U(Reserved)	---	RC72
Pentium/Celeron	RC69	---
I3/I5/I7	RC71	---



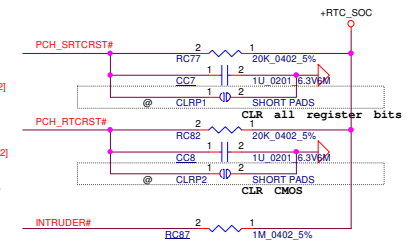
RC200,RC201	DIS/UMA SKU Opt i on d
LOW(DEFAULT)	UMA
HIGH	DIS

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Size	Document Number	Rev
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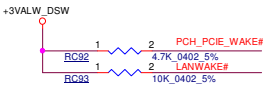
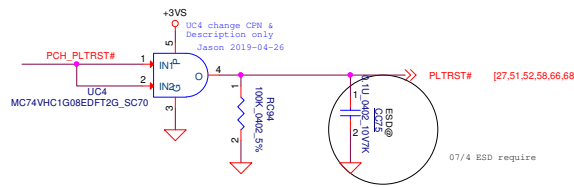
## RC78,RC81,RC85,RC88 close to Device



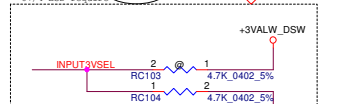
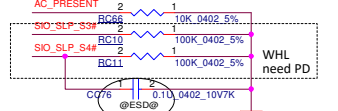
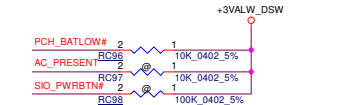
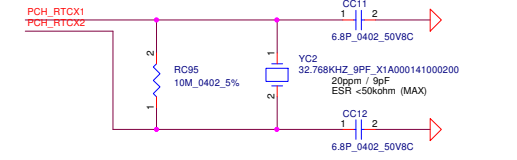
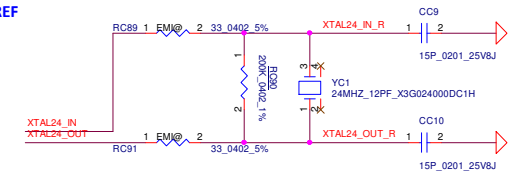
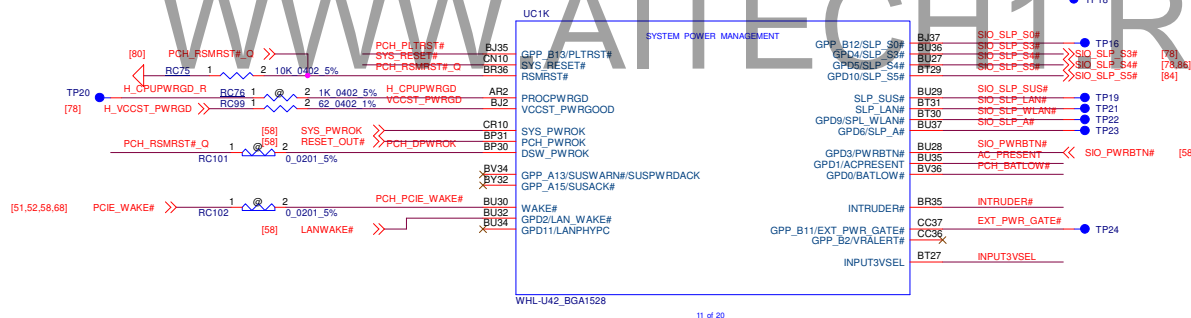
**COMPENSATION FOR XCLK\_BIASREF**  
CAD Note:  
Min trace width=10 mils, Spacing=15 mils  
Max trace length=1000 mils



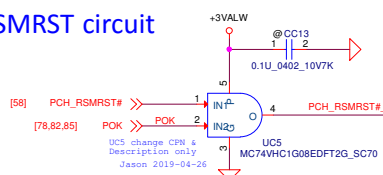
## PCH\_PLTRST#



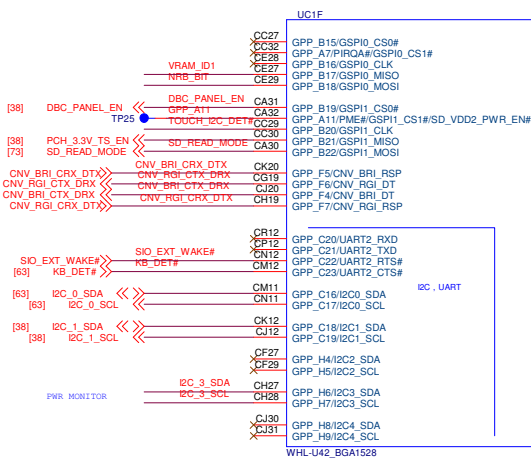
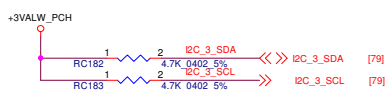
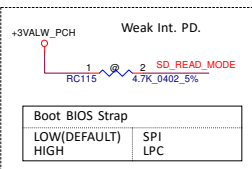
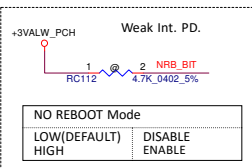
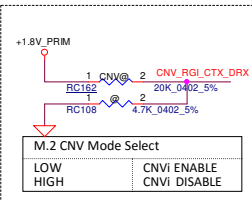
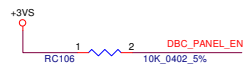
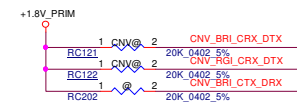
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## RSMRST circuit

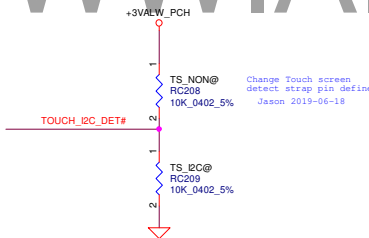


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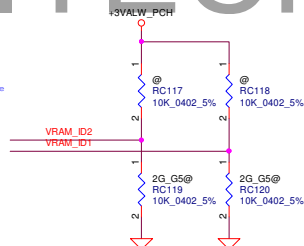


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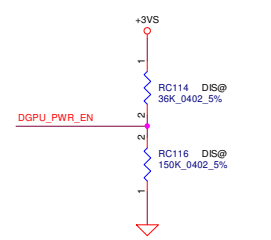
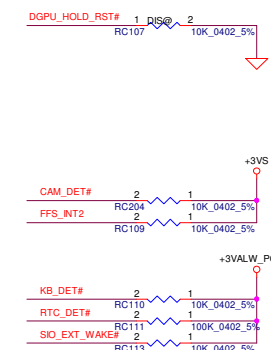


RC208,RC209 Touch panel interface	
LOW	I2C
HIGH	USB



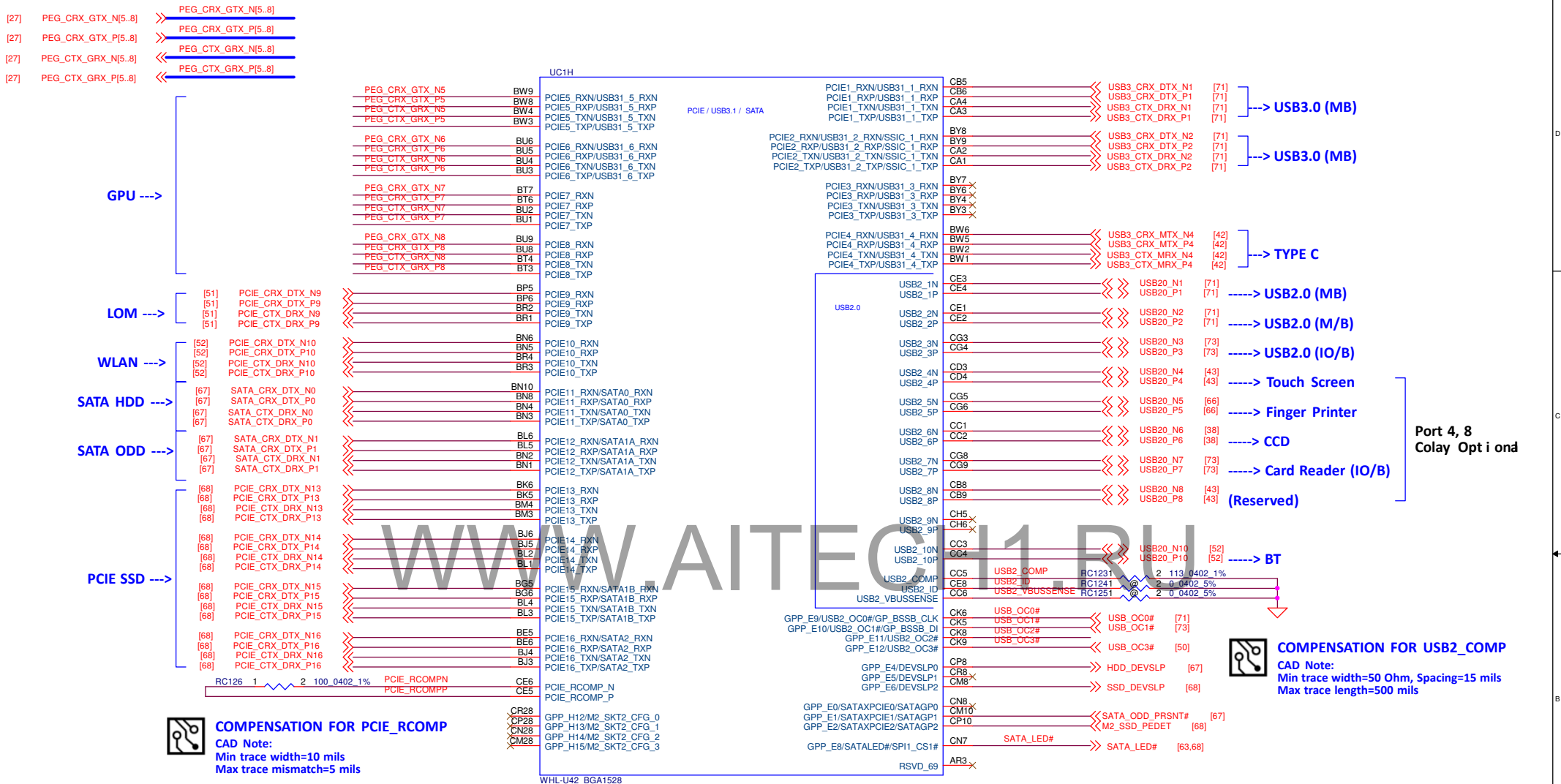
VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

\*Combine in X76



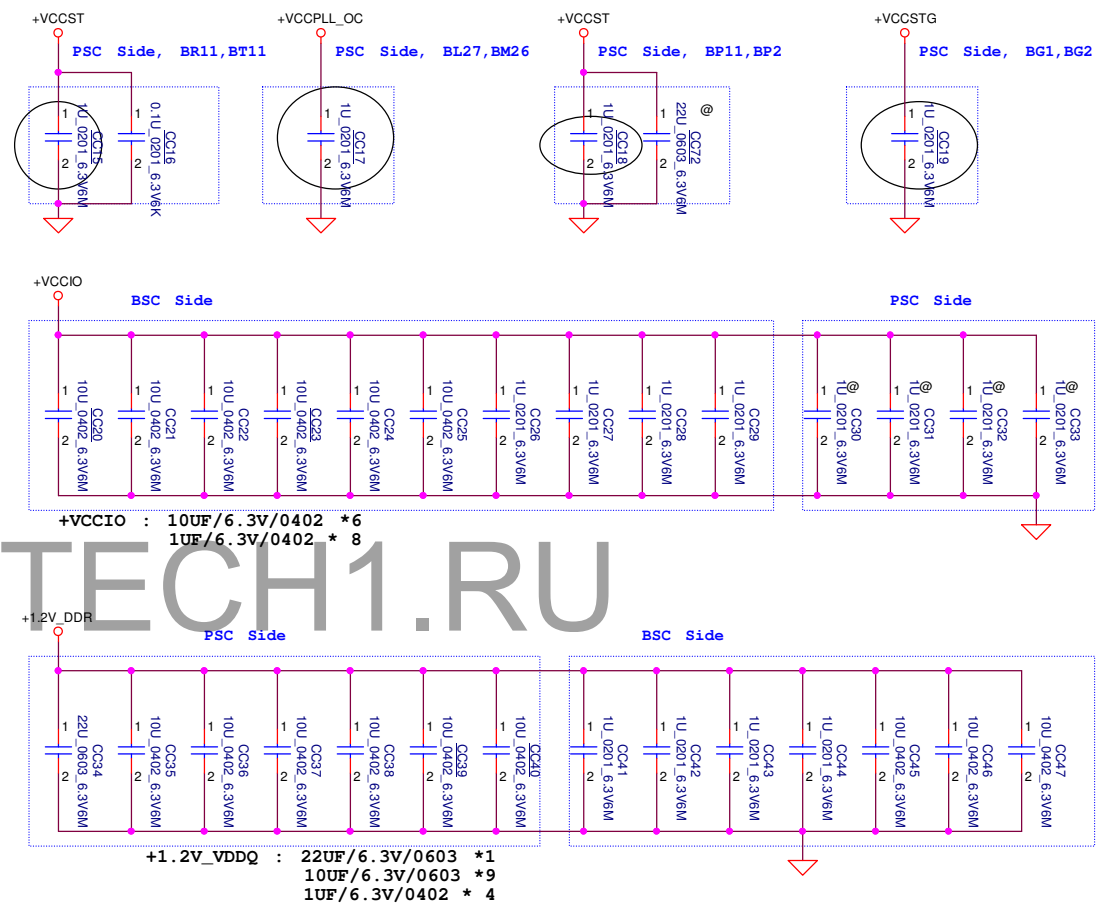
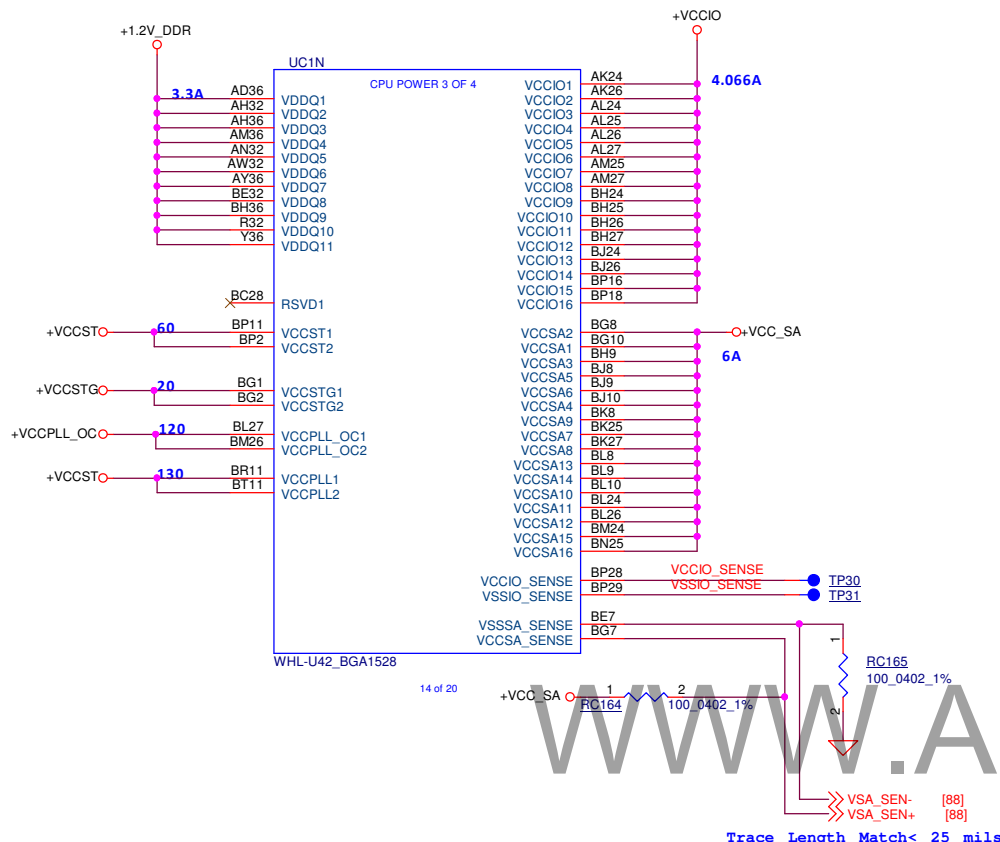
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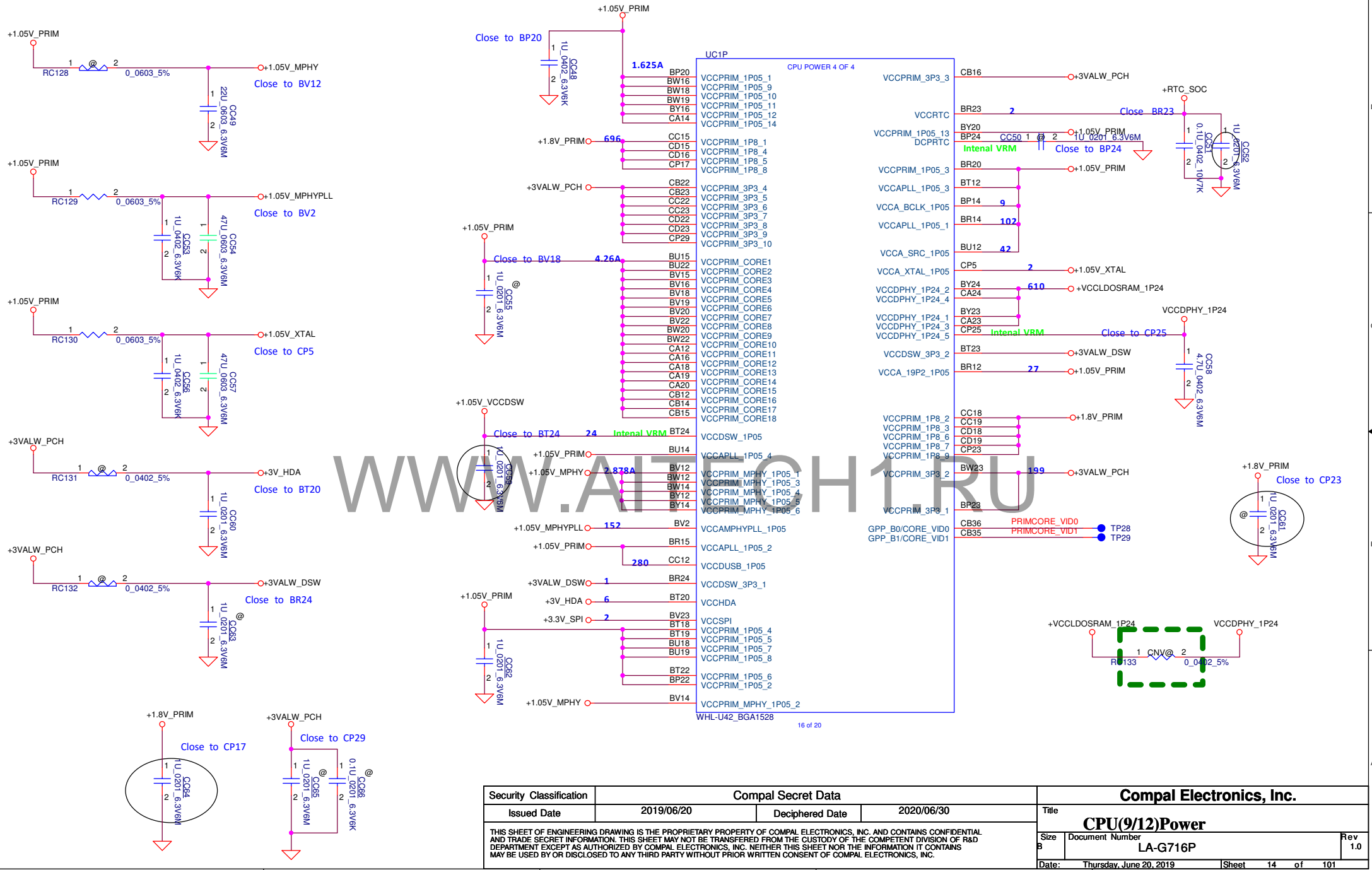


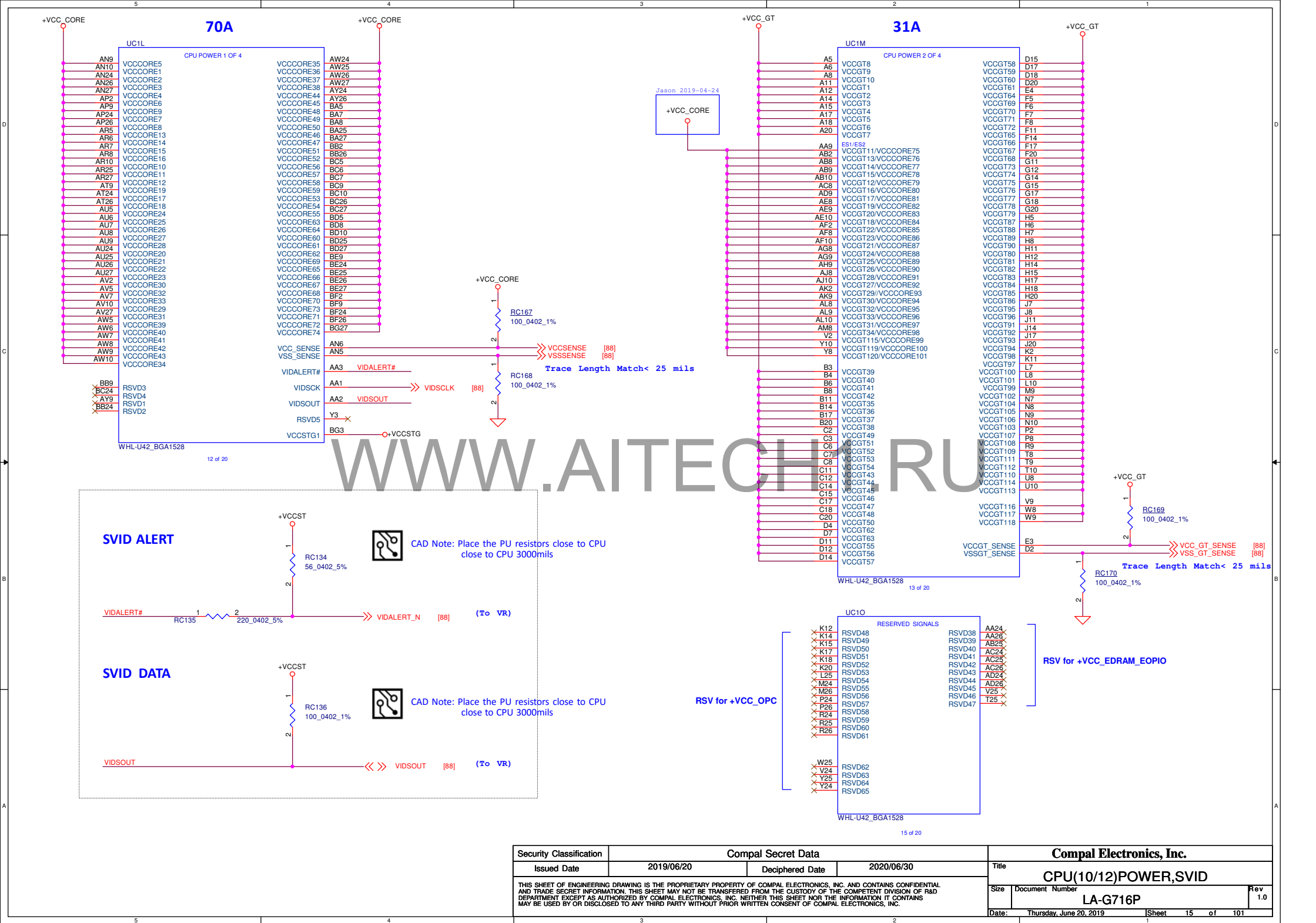
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						Size		Document Number		Rev	
						Custom		LA-G716P		1.0	
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						3		1		2	

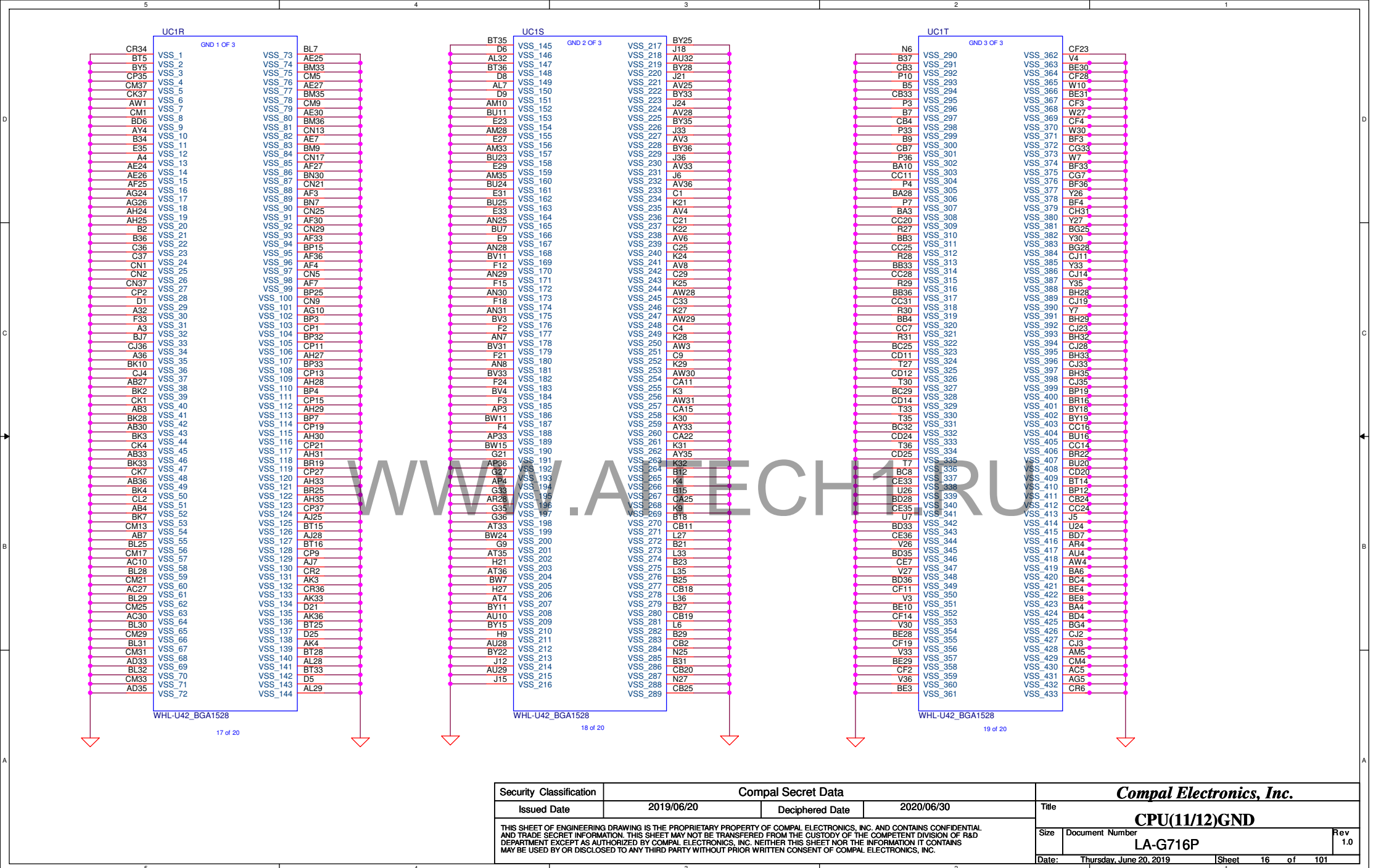




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				Size	Rev
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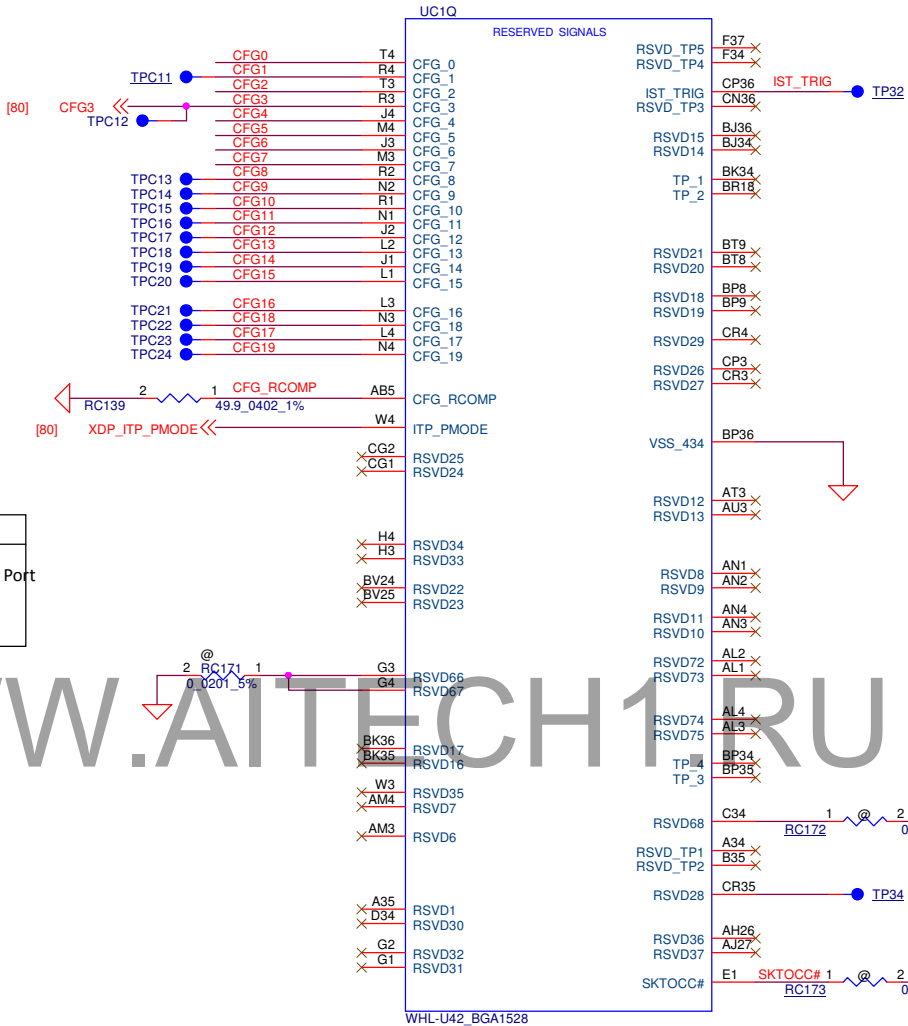
Reset sequence after PCU PLL is locked	
CFG0	1 : (DEFAULT) Normal Operation No Stall 0 : Stall

PCI Express Static Lane Reversal For All PEG Ports	
CFG2	1 : (DEFAULT) Normal Operation 0 : Lane Reversal

Display Port Presence Strap	
CFG4	0 : Enabled; An external Display Port device is connected to the Embedded Display Port 1 : Disabled; No Physical Display Port attached to Embedded Display Port

PCI Express Bifurcation	
CFG[6:5]	<ul style="list-style-type: none"> <li>00 = 1x8 2x4 PCI Express*</li> <li>01 = reserved</li> <li>10 = 2x8 PCI Express*</li> <li>11 = 1x16 PCI Express*</li> </ul>

PEG Training	
CFG7	1 : (default) PEG Train immediately following RESET# de-assertion 0 : PEG Wait for BIOS for training.



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Main Function:

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Main Function:

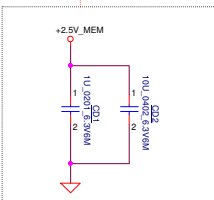
# Reserve

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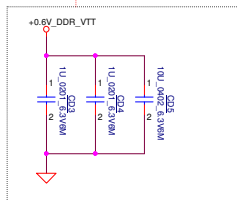
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Main Func = DDR

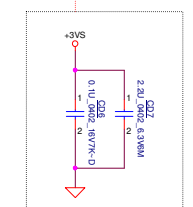
Layout Note:  
Place near JDIMM1.257,259



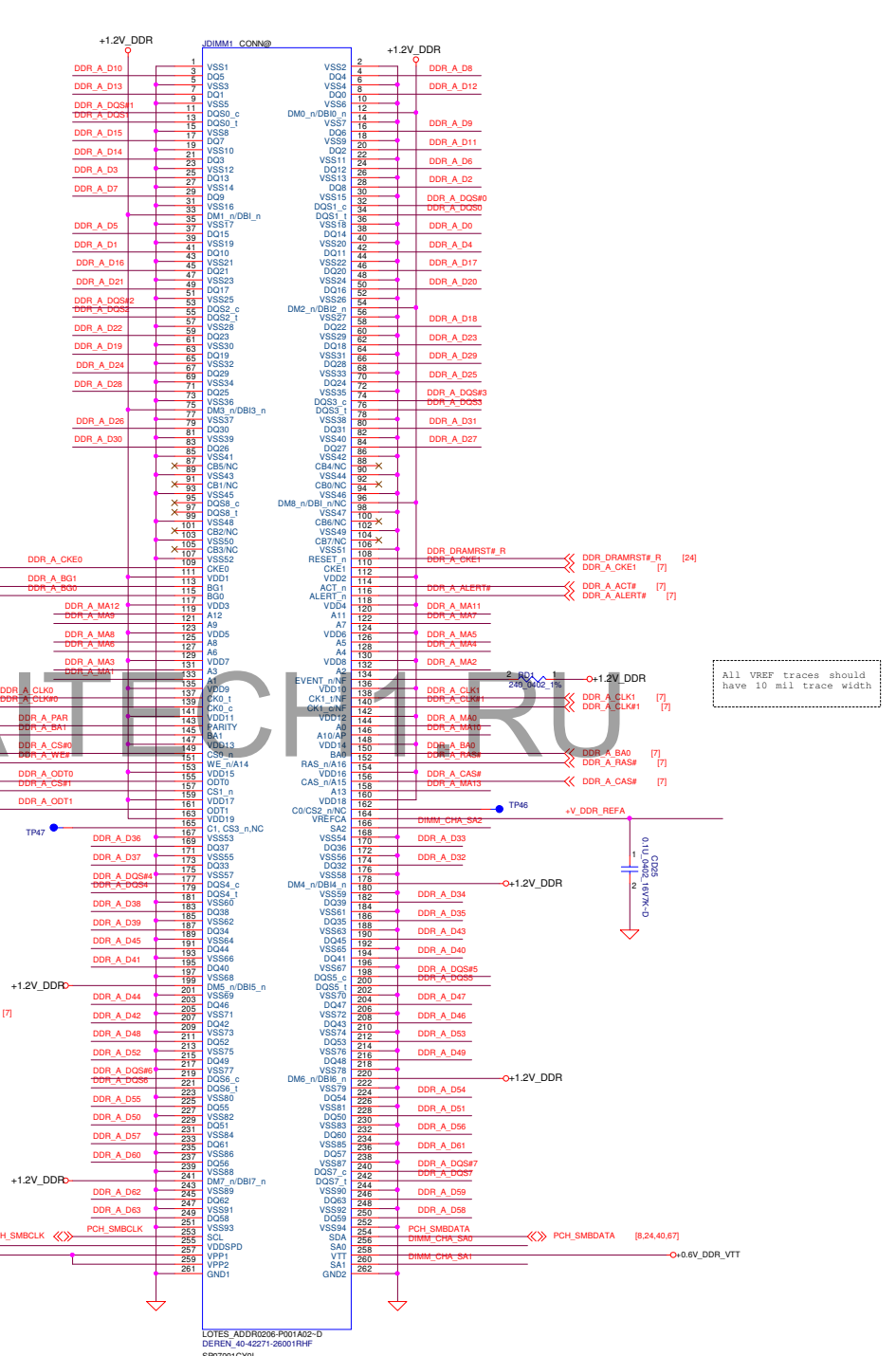
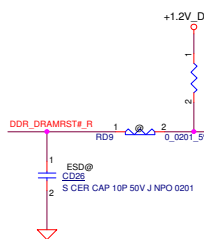
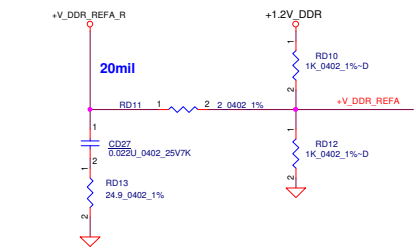
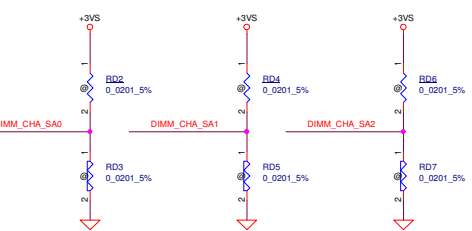
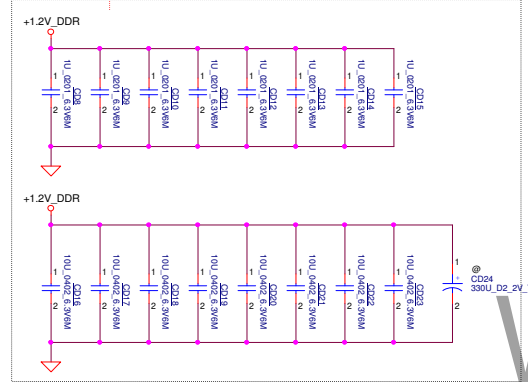
Layout Note:  
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Layout Note:  
Place near JDIMM1.255



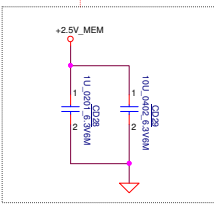
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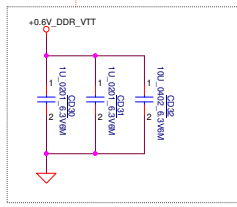
All VREF traces should  
have 10 mil trace width

Main Func = DDR

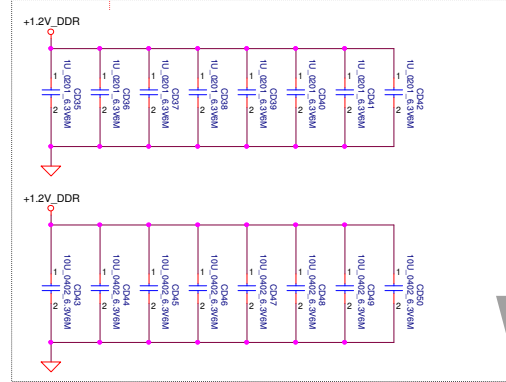
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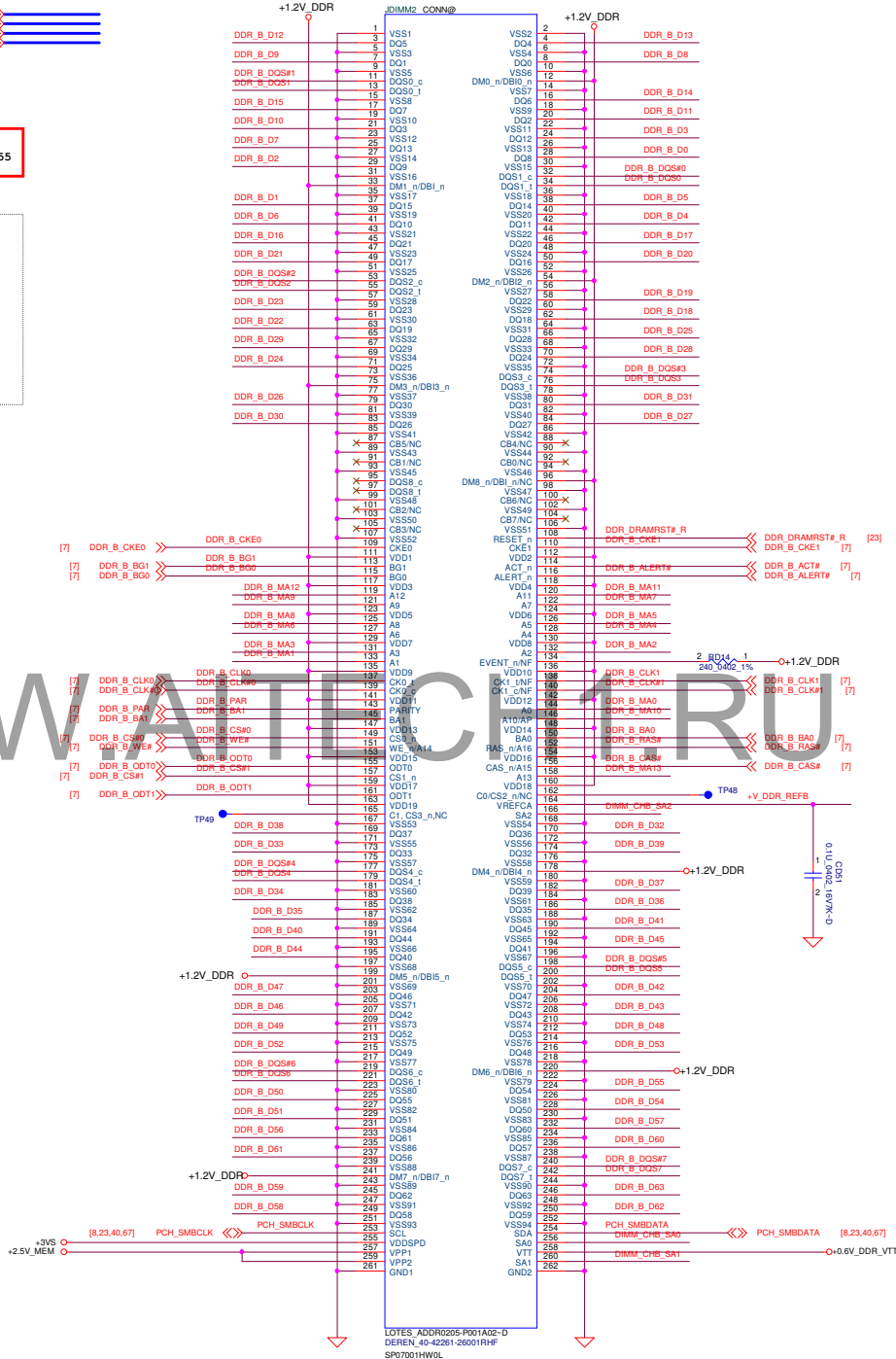
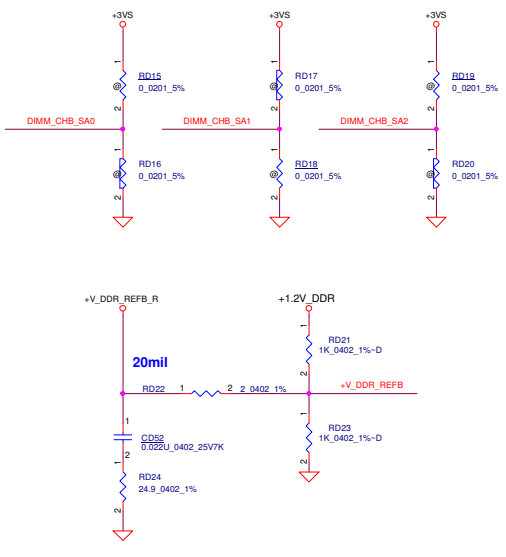
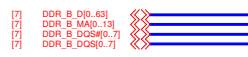
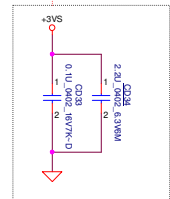
Layout Note:  
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Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIMM2.255



All VREF traces should  
have 10 mil trace width

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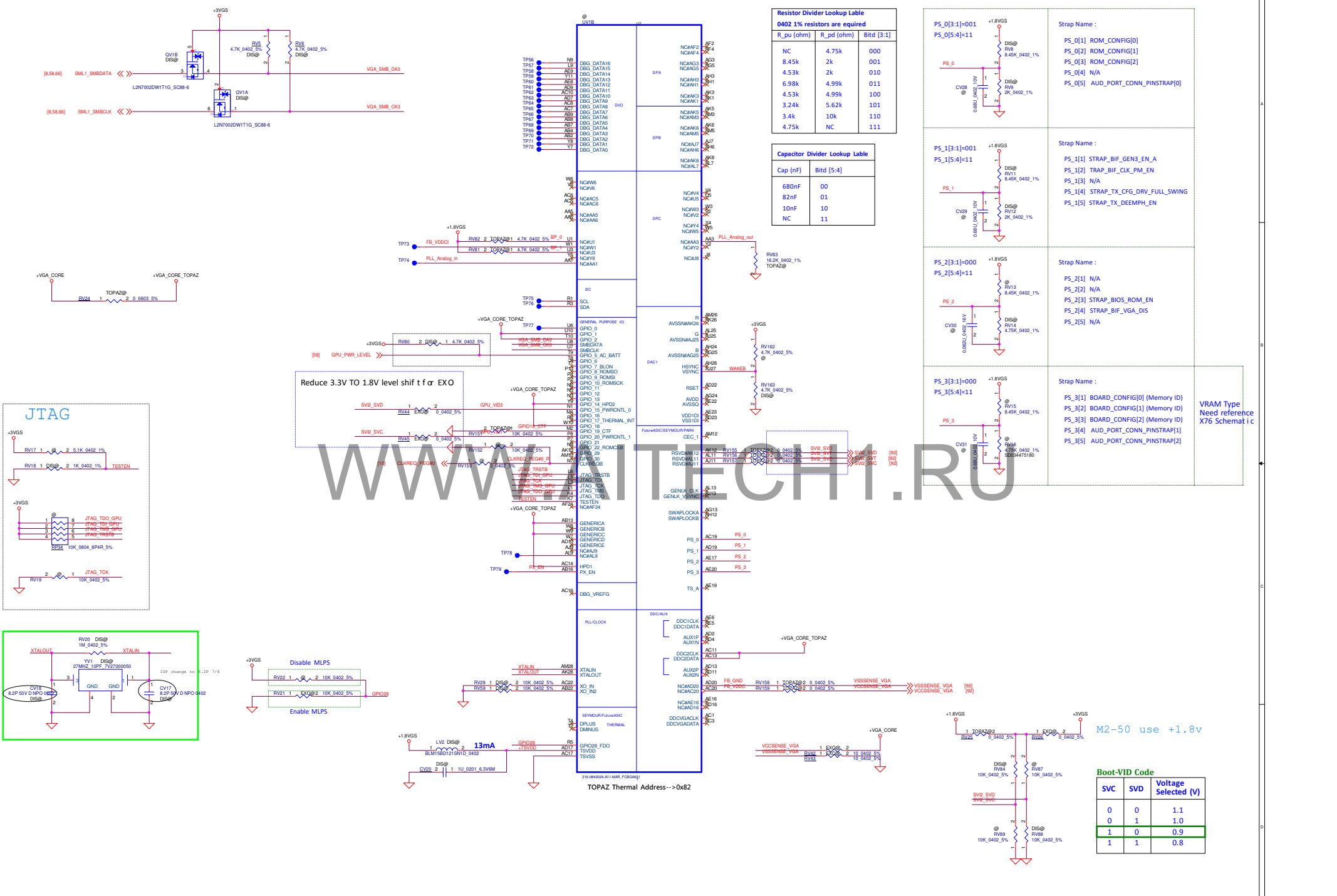
Main Function:

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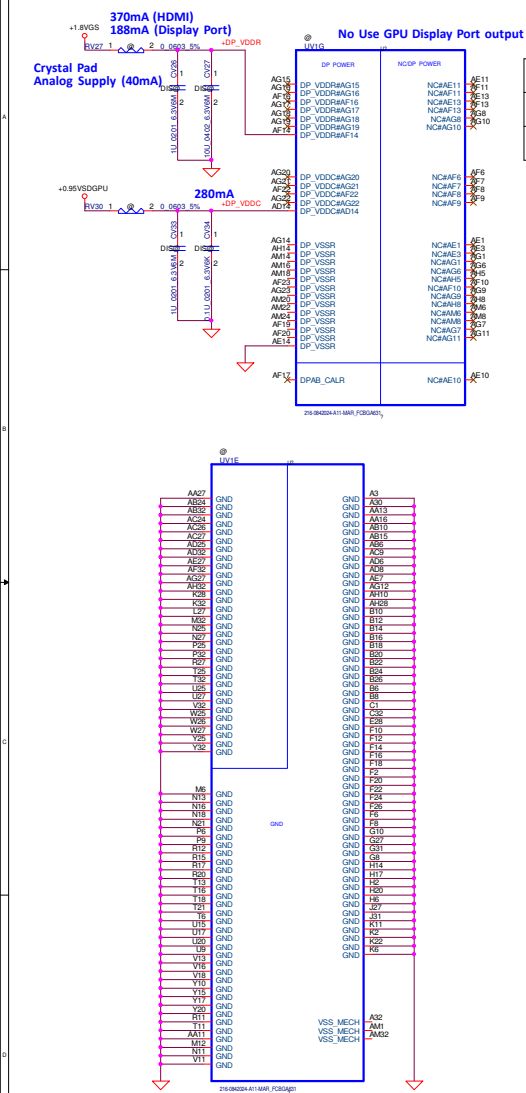
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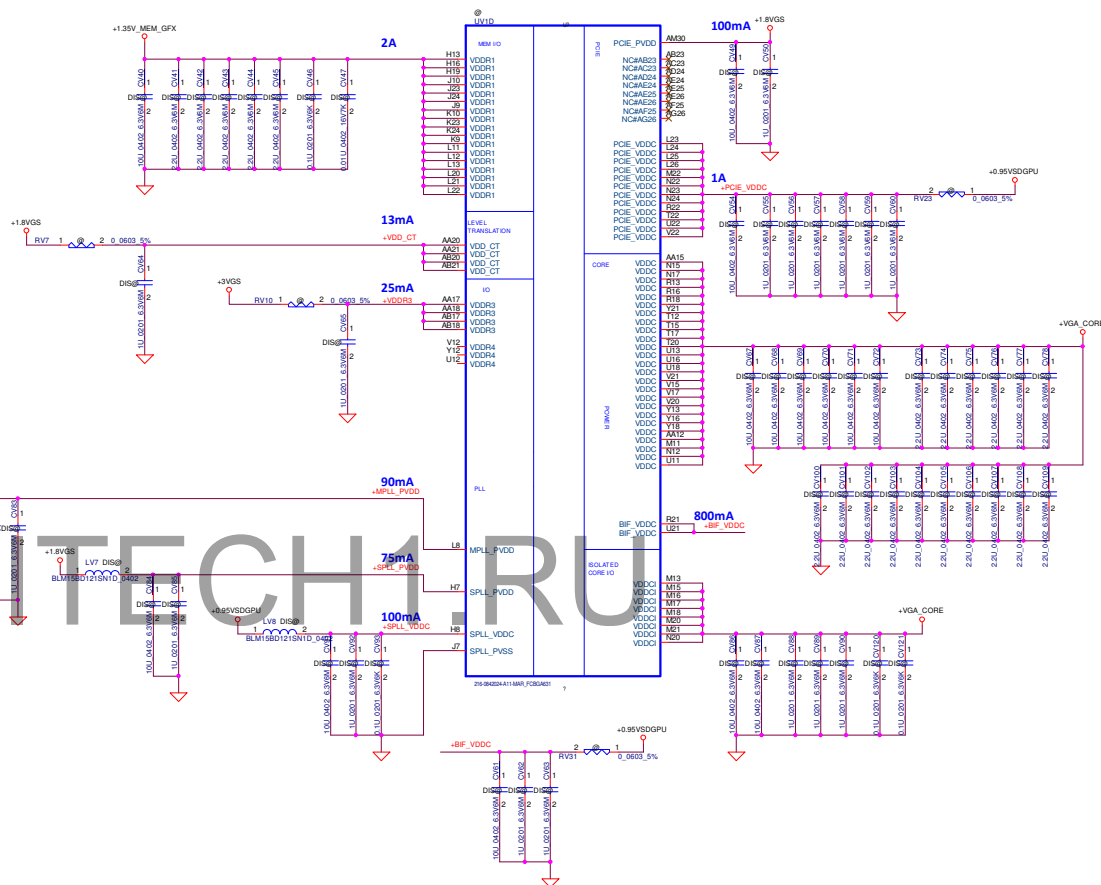
+VGA_CORE	10uF	2.2uF	0.1uF
VDDC	6	16	0
VDDCI	2	3	2

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	1	6	0
BIF_VDDC	1	2	0
SPLL_VDDC	1	1	1
+DP_VDDC	0	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	1	5	1	1

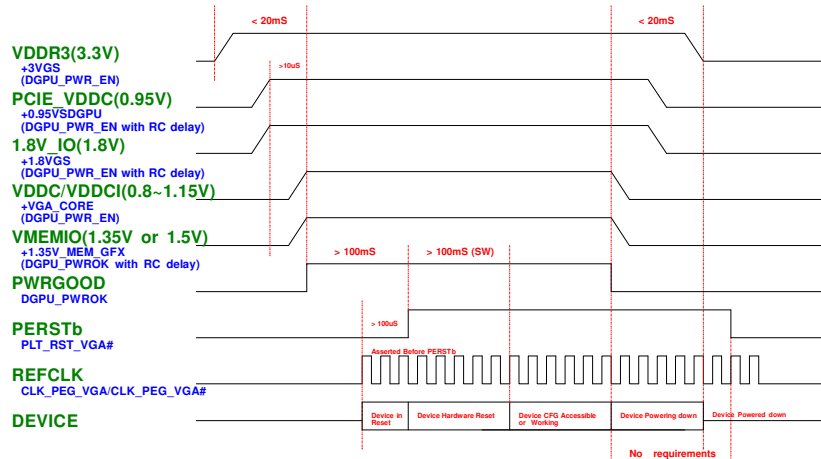
+3VGS	10uF	1uF	0.1uF
VDDR3	0	1	0

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	1	1	0
MPPLL_PVDD	2	1	0
SPLL_PVDD	1	1	0
VDDR4 (NC)	0	0	0
VDD_CT	0	1	0
+TSVDD	0	1	0
+DP_VDDR	1	1	0

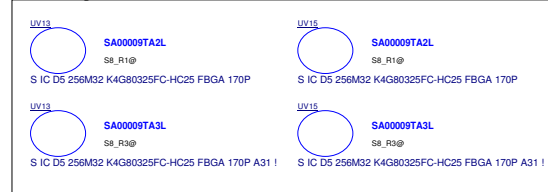


## Power-Up/Down Sequence

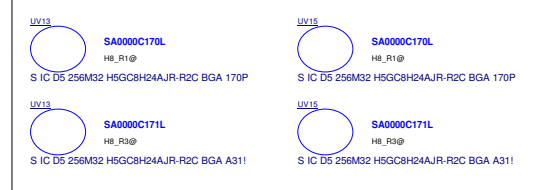
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as 50 mV/ $\mu$ s).
5. VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.



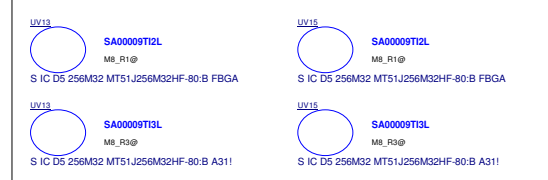
## Samsung 2G



## Hynix 2G



## Micron 2G



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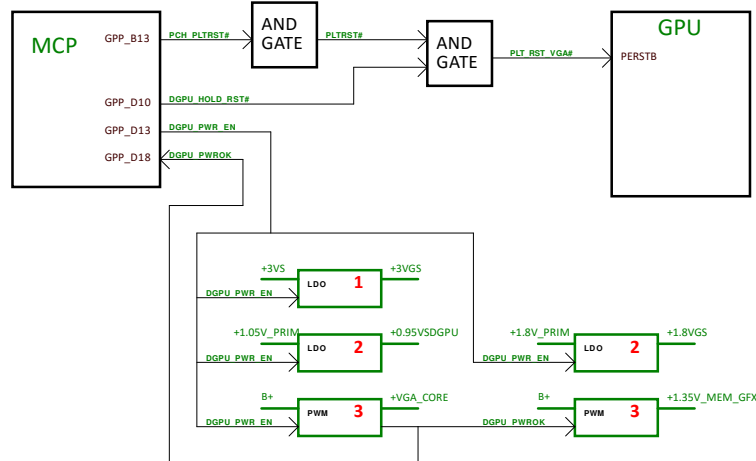
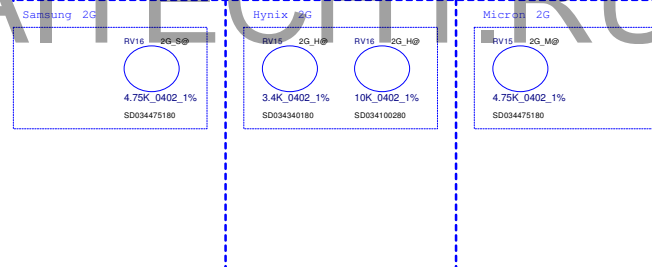


Table 3-21 Resistor Divider Lookup T.

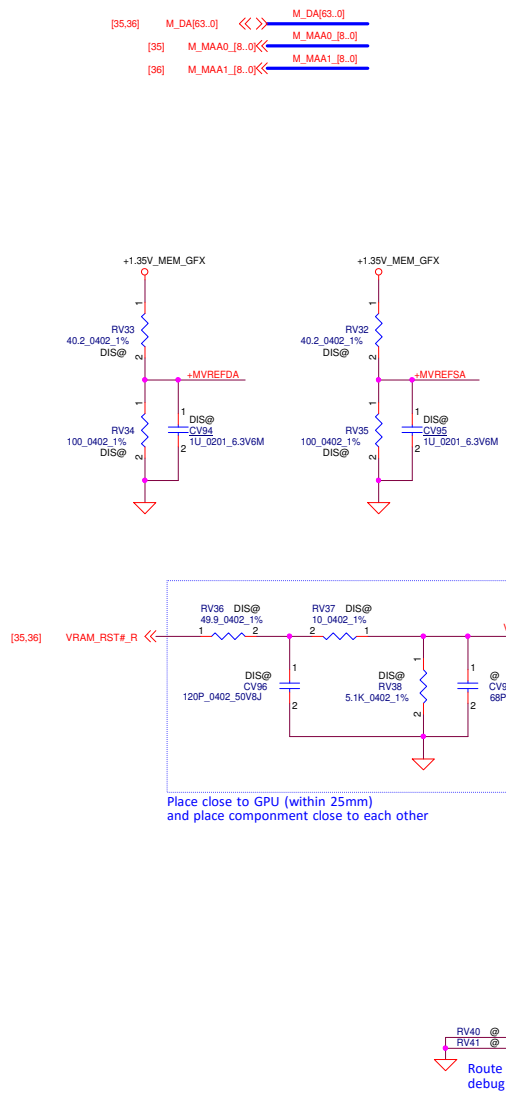
R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

## For AMD R17M-M1-30 VRAM

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TA3L	SAMSUNG	S IC D5 256M32 K4G80325FC-HC25 FBGA 170P A31 !	2GB
110	SA0000C171L	Hynix	S IC D5 256M32 H5GC8H24AJR-R2C BGA A31!	2GB
111	SA00009T13L	Micron	S IC D5 256M32 MT51J256M32HF-80:B A31!	2GB

Main Func = GPU



M_DA0		M_DAA0		M_MAA1	
M_DA0	K27	M_DAA0	K27	M_MAA1	K27
M_DA1	J29	M_DAA1	J29	M_MAA1	J29
M_DA2	H30	M_DAA2	H30	M_MAA1	H30
M_DA3	H32	M_DAA3	H32	M_MAA1	H32
M_DA4	G29	M_DAA4	G29	M_MAA1	G29
M_DA5	F32	M_DAA5	F32	M_MAA1	F32
M_DA6	F30	M_DAA6	F30	M_MAA1	F30
M_DA7	C30	M_DAA7	C30	M_MAA1	C30
M_DA8	A28	M_DAA8	A28	M_MAA1	A28
M_DA9	A28	M_DAA9	A28	M_MAA1	A28
M_DA10	C28	M_DAA10	C28	M_MAA1	C28
M_DA11	C27	M_DAA11	C27	M_MAA1	C27
M_DA12	G26	M_DAA12	G26	M_MAA1	G26
M_DA13	D26	M_DAA13	D26	M_MAA1	D26
M_DA14	F25	M_DAA14	F25	M_MAA1	F25
M_DA15	A25	M_DAA15	A25	M_MAA1	A25
M_DA16	C25	M_DAA16	C25	M_MAA1	C25
M_DA17	E25	M_DAA17	E25	M_MAA1	E25
M_DA18	D24	M_DAA18	D24	M_MAA1	D24
M_DA19	E23	M_DAA19	E23	M_MAA1	E23
M_DA20	F23	M_DAA20	F23	M_MAA1	F23
M_DA21	D22	M_DAA21	D22	M_MAA1	D22
M_DA22	F21	M_DAA22	F21	M_MAA1	F21
M_DA23	E21	M_DAA23	E21	M_MAA1	E21
M_DA24	D20	M_DAA24	D20	M_MAA1	D20
M_DA25	F19	M_DAA25	F19	M_MAA1	F19
M_DA26	A19	M_DAA26	A19	M_MAA1	A19
M_DA27	D18	M_DAA27	D18	M_MAA1	D18
M_DA28	E17	M_DAA28	E17	M_MAA1	E17
M_DA29	A17	M_DAA29	A17	M_MAA1	A17
M_DA30	C17	M_DAA30	C17	M_MAA1	C17
M_DA31	E17	M_DAA31	E17	M_MAA1	E17
M_DA32	D16	M_DAA32	D16	M_MAA1	D16
M_DA33	F15	M_DAA33	F15	M_MAA1	F15
M_DA34	A15	M_DAA34	A15	M_MAA1	A15
M_DA35	D14	M_DAA35	D14	M_MAA1	D14
M_DA36	F13	M_DAA36	F13	M_MAA1	F13
M_DA37	A13	M_DAA37	A13	M_MAA1	A13
M_DA38	C13	M_DAA38	C13	M_MAA1	C13
M_DA39	E11	M_DAA39	E11	M_MAA1	E11
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M_DA41	C11	M_DAA41	C11	M_MAA1	C11
M_DA42	F11	M_DAA42	F11	M_MAA1	F11
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M_DA44	C9	M_DAA44	C9	M_MAA1	C9
M_DA45	E9	M_DAA45	E9	M_MAA1	E9
M_DA46	A7	M_DAA46	A7	M_MAA1	A7
M_DA47	C7	M_DAA47	C7	M_MAA1	C7
M_DA48	E7	M_DAA48	E7	M_MAA1	E7
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M_DA50	C7	M_DAA50	C7	M_MAA1	C7
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M_DA52	A5	M_DAA52	A5	M_MAA1	A5
M_DA53	E5	M_DAA53	E5	M_MAA1	E5
M_DA54	C3	M_DAA54	C3	M_MAA1	C3
M_DA55	E1	M_DAA55	E1	M_MAA1	E1
M_DA56	G1	M_DAA56	G1	M_MAA1	G1
M_DA57	H1	M_DAA57	H1	M_MAA1	H1
M_DA58	J1	M_DAA58	J1	M_MAA1	J1
M_DA59	K1	M_DAA59	K1	M_MAA1	K1
M_DA60	L1	M_DAA60	L1	M_MAA1	L1
M_DA61	M1	M_DAA61	M1	M_MAA1	M1
M_DA62	N1	M_DAA62	N1	M_MAA1	N1
M_DA63	P1	M_DAA63	P1	M_MAA1	P1
M_DA64	Q1	M_DAA64	Q1	M_MAA1	Q1
M_DA65	R1	M_DAA65	R1	M_MAA1	R1
M_DA66	S1	M_DAA66	S1	M_MAA1	S1
M_DA67	T1	M_DAA67	T1	M_MAA1	T1
M_DA68	U1	M_DAA68	U1	M_MAA1	U1
M_DA69	V1	M_DAA69	V1	M_MAA1	V1
M_DA70	W1	M_DAA70	W1	M_MAA1	W1
M_DA71	X1	M_DAA71	X1	M_MAA1	X1
M_DA72	Y1	M_DAA72	Y1	M_MAA1	Y1
M_DA73	Z1	M_DAA73	Z1	M_MAA1	Z1
M_DA74	AA1	M_DAA74	AA1	M_MAA1	AA1
M_DA75	AB1	M_DAA75	AB1	M_MAA1	AB1
M_DA76	AC1	M_DAA76	AC1	M_MAA1	AC1
M_DA77	AD1	M_DAA77	AD1	M_MAA1	AD1
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M_DA82	AI1	M_DAA82	AI1	M_MAA1	AI1
M_DA83	AJ1	M_DAA83	AJ1	M_MAA1	AJ1
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M_DA86	AM1	M_DAA86	AM1	M_MAA1	AM1
M_DA87	AN1	M_DAA87	AN1	M_MAA1	AN1
M_DA88	AO1	M_DAA88	AO1	M_MAA1	AO1
M_DA89	AP1	M_DAA89	AP1	M_MAA1	AP1
M_DA90	AQ1	M_DAA90	AQ1	M_MAA1	AQ1
M_DA91	AR1	M_DAA91	AR1	M_MAA1	AR1
M_DA92	AS1	M_DAA92	AS1	M_MAA1	AS1
M_DA93	AT1	M_DAA93	AT1	M_MAA1	AT1
M_DA94	AU1	M_DAA94	AU1	M_MAA1	AU1
M_DA95	AV1	M_DAA95	AV1	M_MAA1	AV1
M_DA96	AW1	M_DAA96	AW1	M_MAA1	AW1
M_DA97	AX1	M_DAA97	AX1	M_MAA1	AX1
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M_DA111	BL1	M_DAA111	BL1	M_MAA1	BL1
M_DA112	BM1	M_DAA112	BM1	M_MAA1	BM1
M_DA113	BN1	M_DAA113	BN1	M_MAA1	BN1
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M_DA115	BP1	M_DAA115	BP1	M_MAA1	BP1
M_DA116	BQ1	M_DAA116	BQ1	M_MAA1	BQ1
M_DA117	BR1	M_DAA117	BR1	M_MAA1	BR1
M_DA118	BS1	M_DAA118	BS1	M_MAA1	BS1
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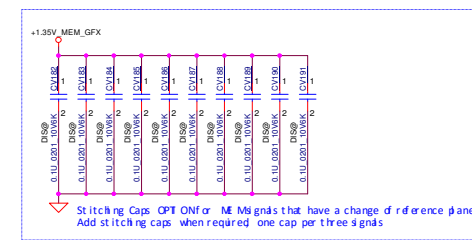
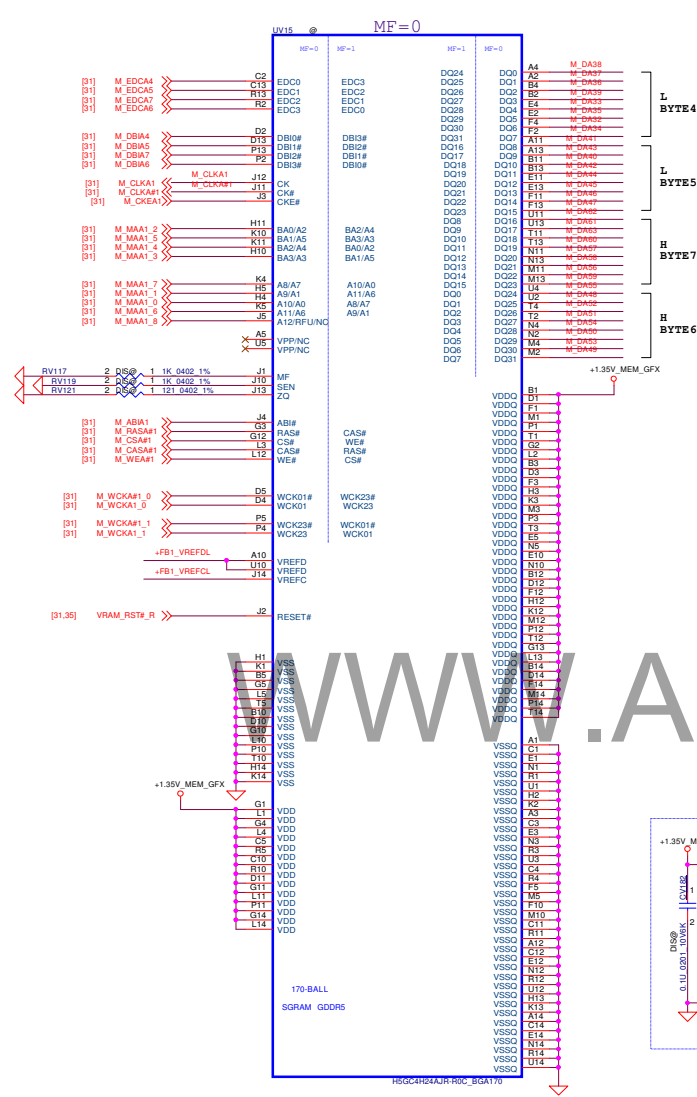
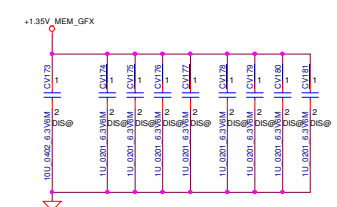
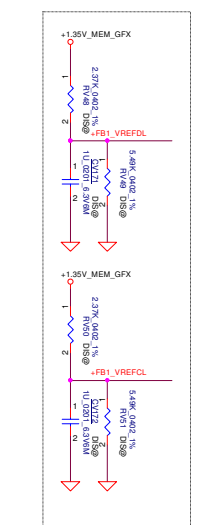
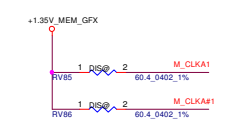
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Main Func = GDDR5

[31] M\_DA[32:63] M\_DA[32:63]



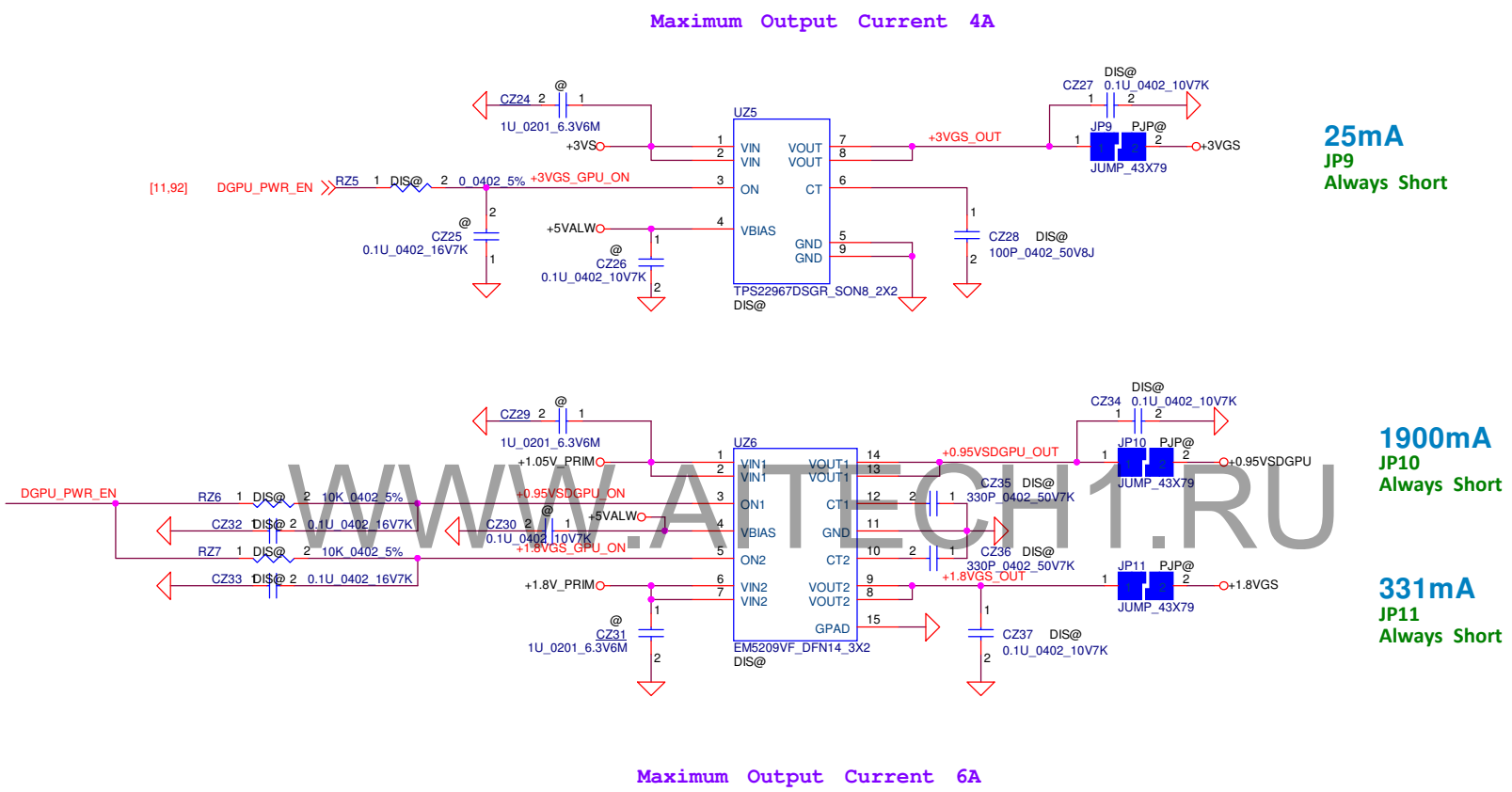
Stitching Caps. OPT ON for M signals that have a change of reference plane voltage  
Add stitching caps when required - one cap per three signals

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Main Func = GPU

+3V/+0.95V/+1.8V for GPU



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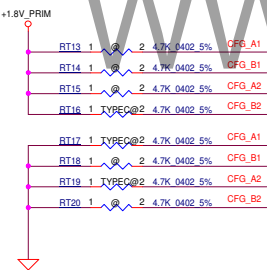


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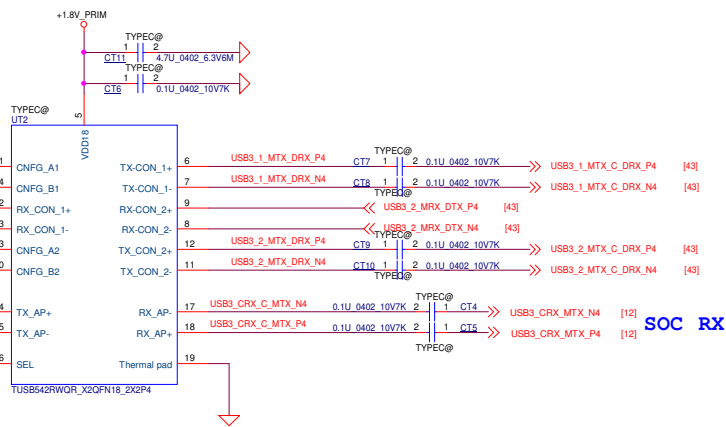
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Main Func = Typec MUX

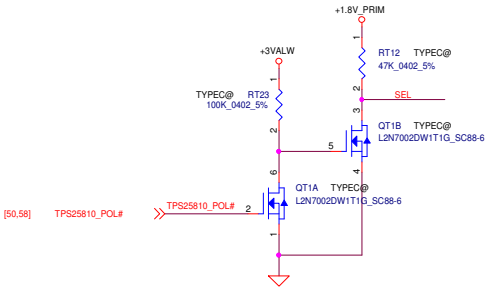


Ultra Low-Power Architecture  
- Active 100 mA  
- U2/U3 1.3 mA  
- No Connection 300  $\mu$  A

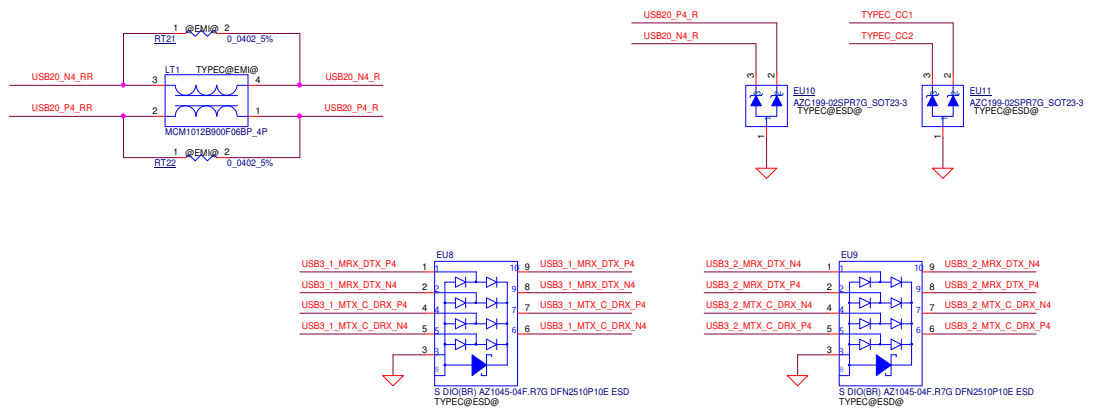
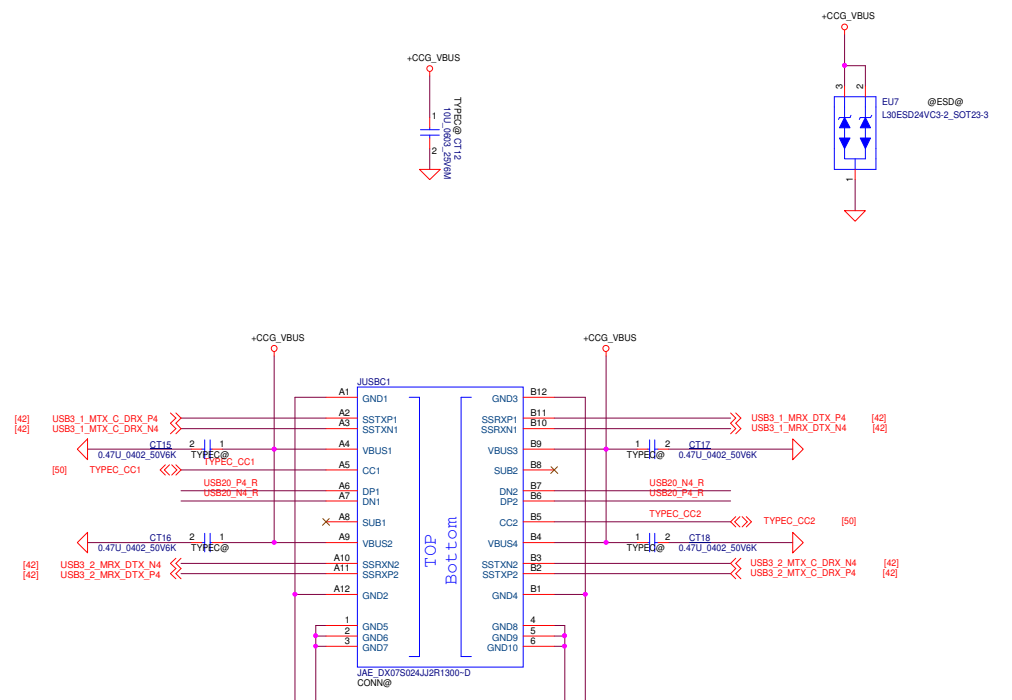
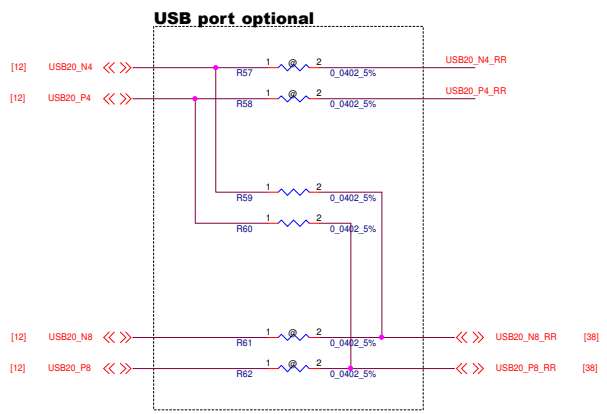


SOC TX

SOC RX



Main Func = USB2 Mux



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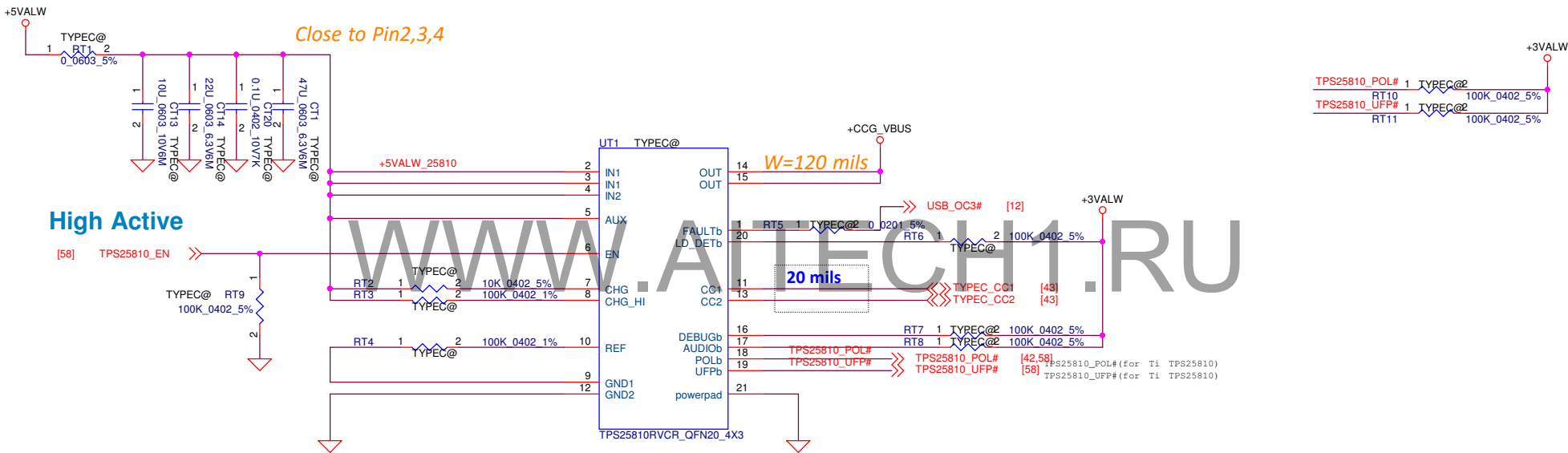
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Main Function: TYPE-C\_Power Path

Main Func = Power Switch

5V@3A



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Main Function: WIGIG / WIDI

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Main Function:

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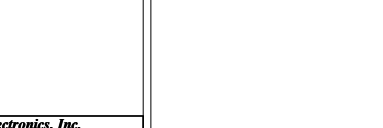
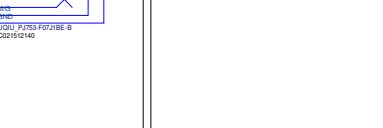
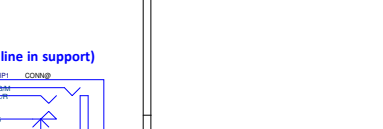
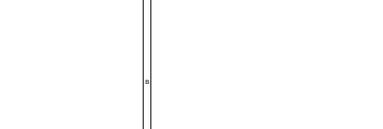
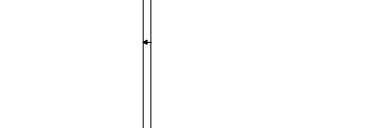
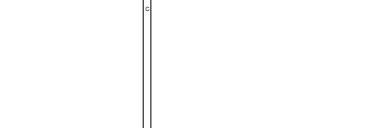
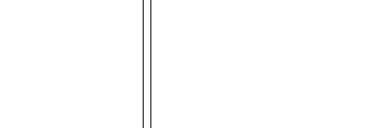
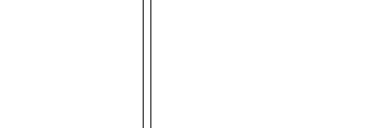
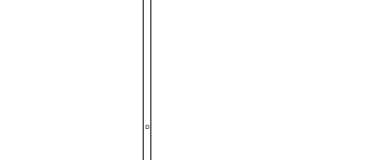
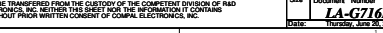
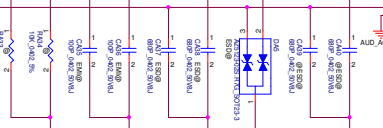
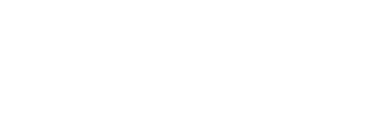
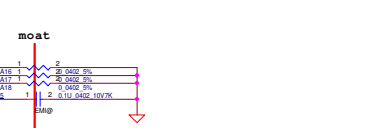
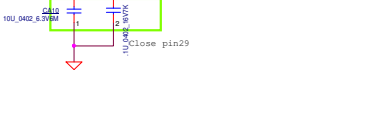
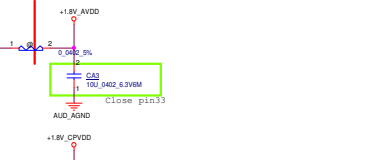
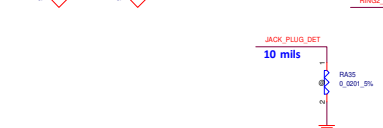
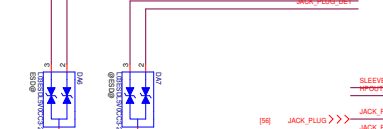
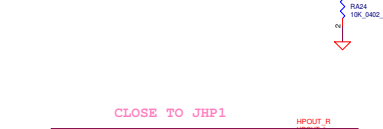
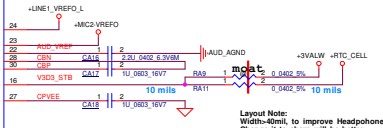
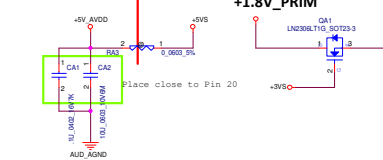
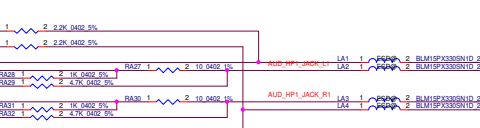
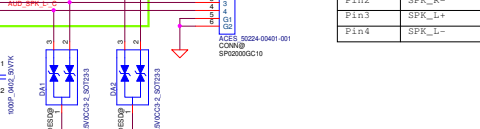
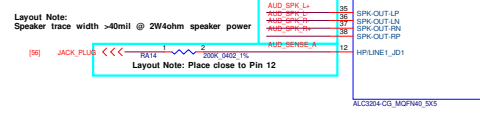
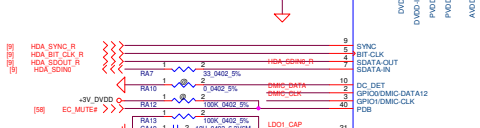
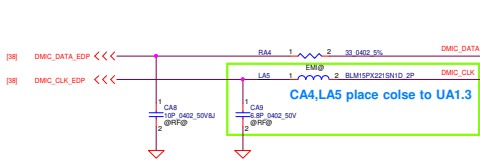
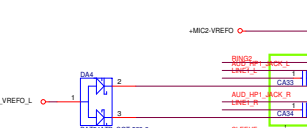
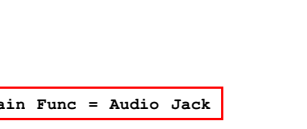
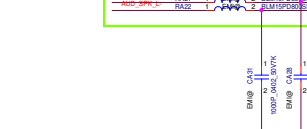
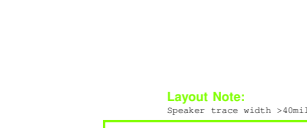
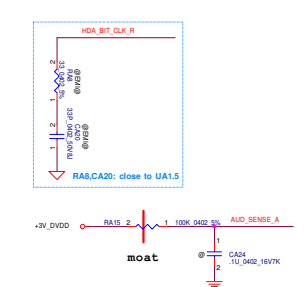
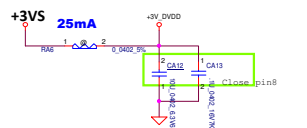
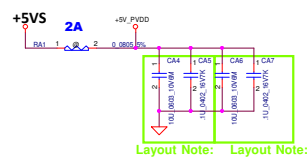
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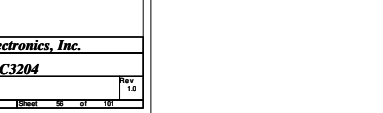
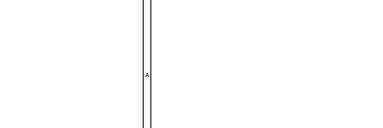
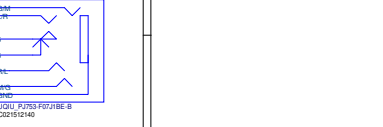
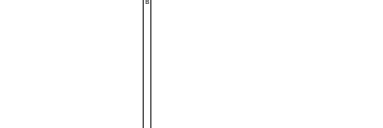
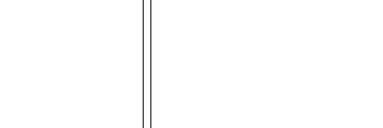
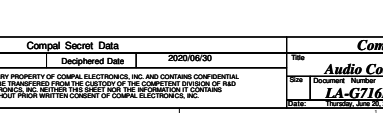
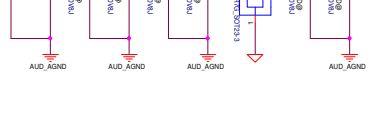
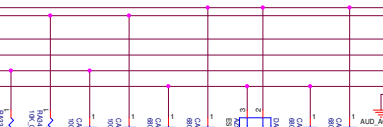
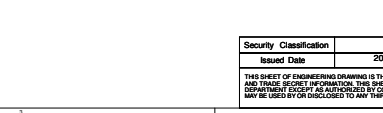
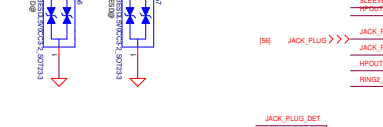
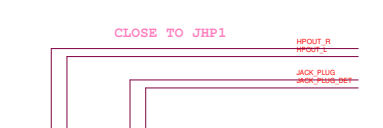
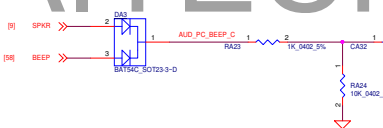
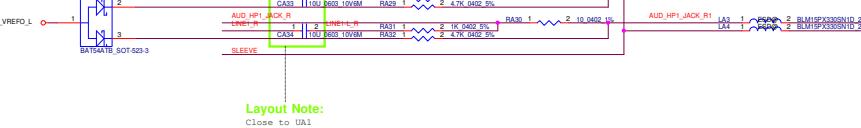
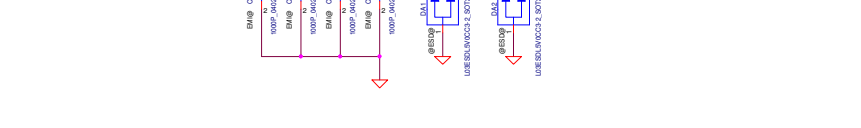
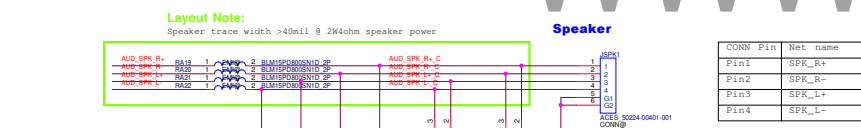
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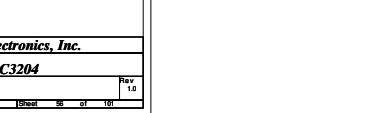
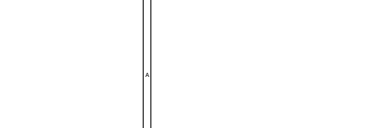
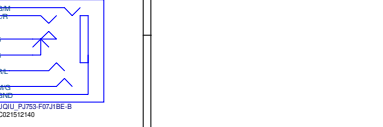
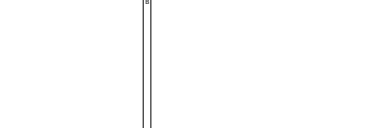
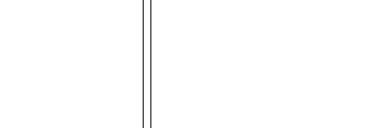
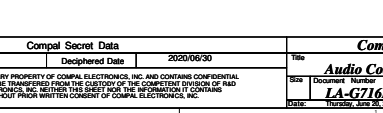
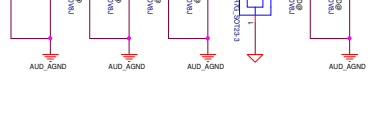
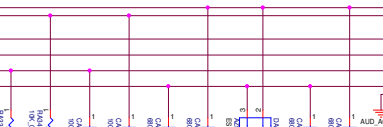
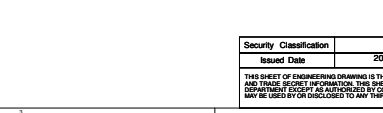
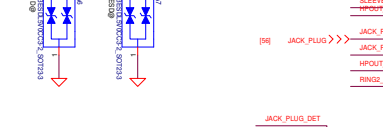
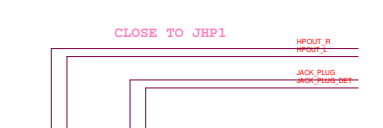
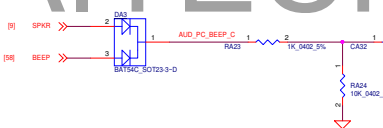
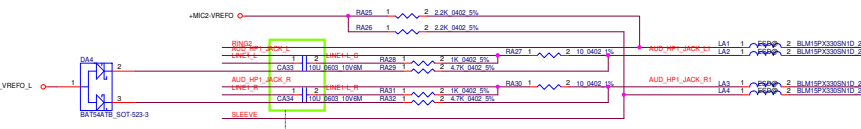


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Main Func = Audio Jack

Universal Jack  
(Global Headset Jack + mic phone in + line in support)

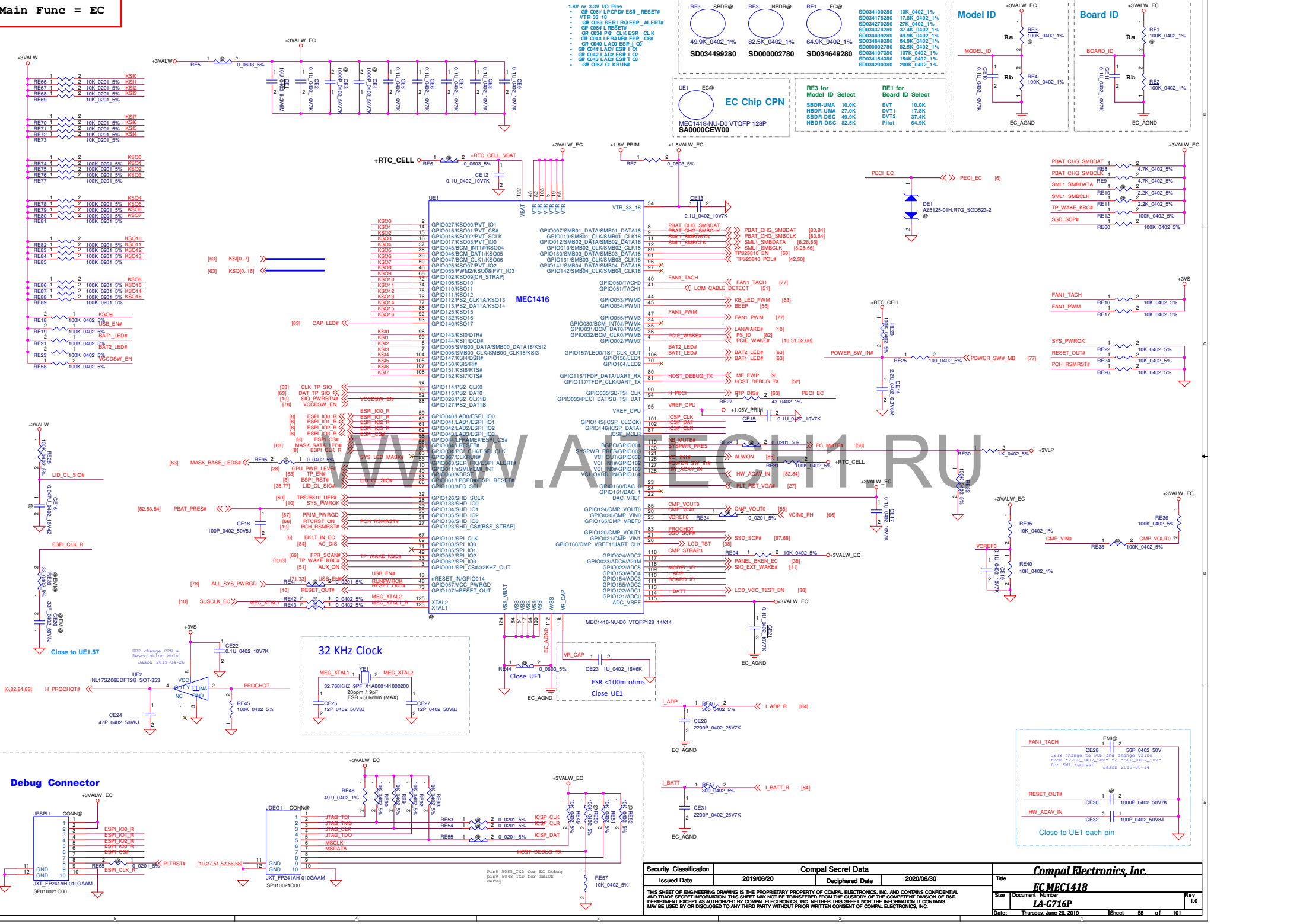


Main Function:

Reserve

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Main Func = EC



Main Function:

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				Size	Document Number
				LA-G716P	
				Date:	Thursday, June 20, 2019
				Sheet	59 of 101
				Rev	1.0

Main Function:

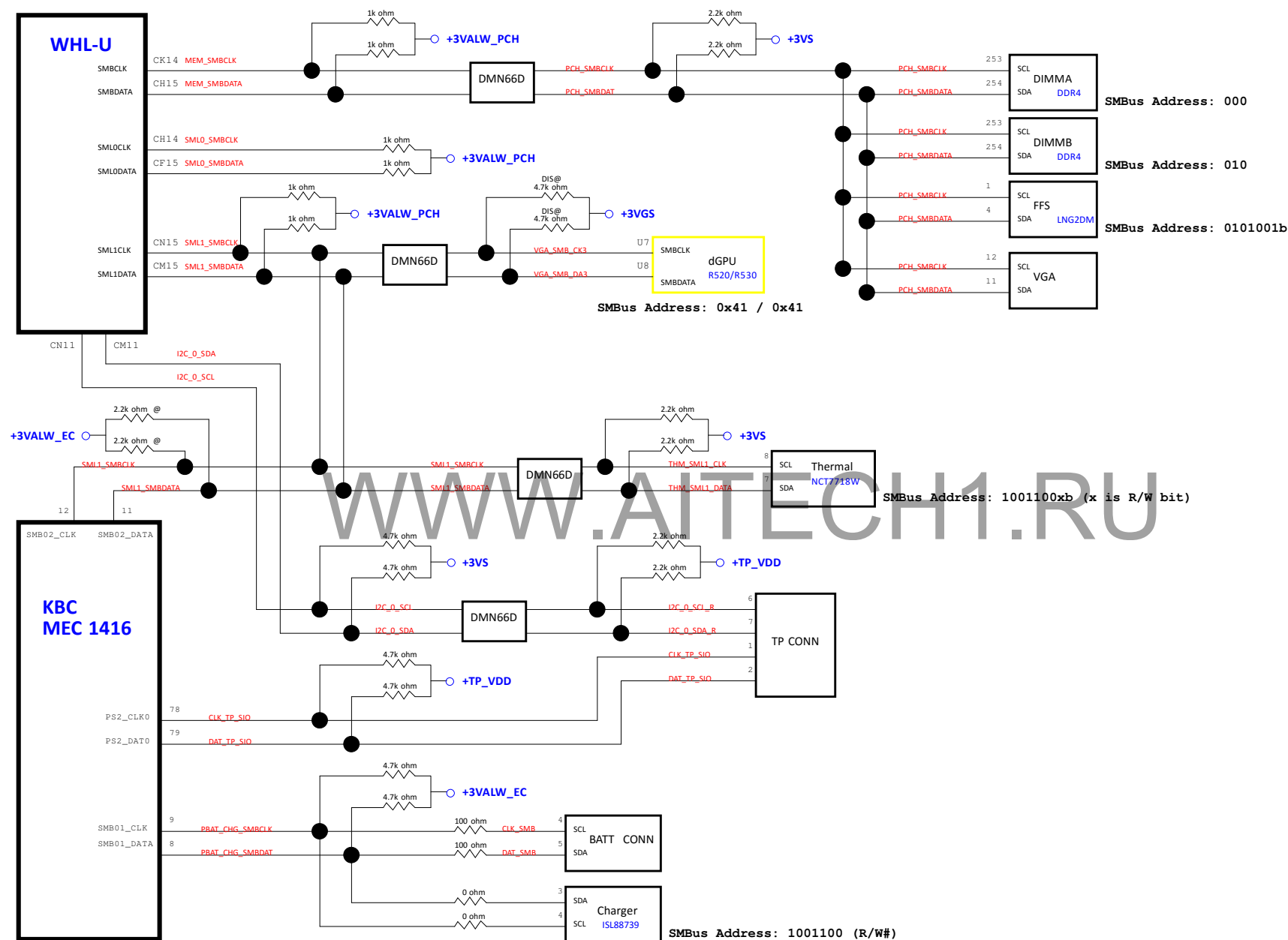
Reserve

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				Size	Rev
				Document Number	1.0
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## Main Function: SMB/I2C Block Diagrams



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				Date:	Thursday, June 20, 2019	Sheet 61 of 101

Main Function:

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				Date:	Thursday, June 20, 2019
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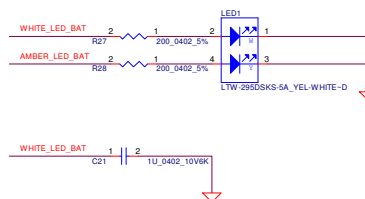
## Main Func = KI



Main Func = Battery LED

Low activated from KBC GPIO

BJT  
R1: 47 K  
R2: 10 K



Main Func = TPA

**EC/PS2**

**PCH/I2C**



Security Classification		Compal Secret Data		Title	
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				Date:	Thursday, June 20, 2019
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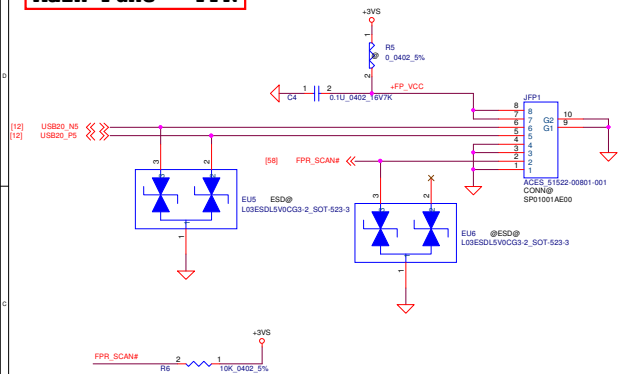
Main Function:

Reserve

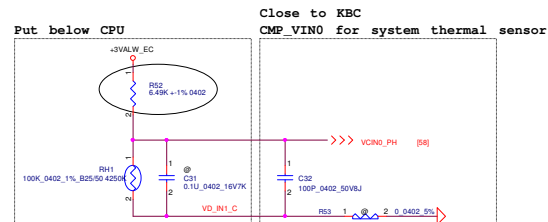
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				Size	Rev
				Document Number	1.0
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				Sheet	65 of 101

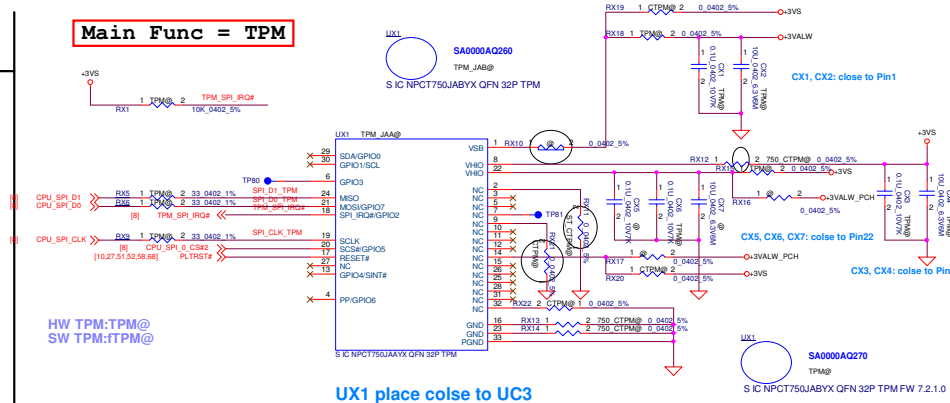
## Main Func = FPR



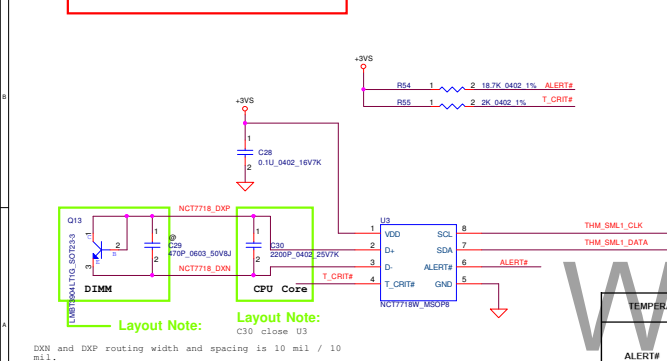
## Main Func = OTP



## Main Func = TPM

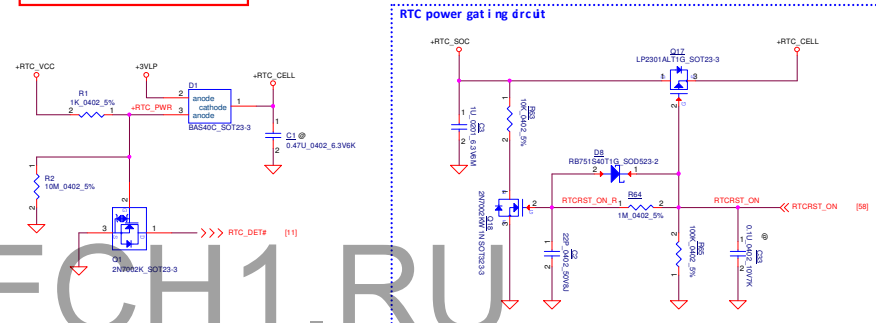


## Main Func = Thermal



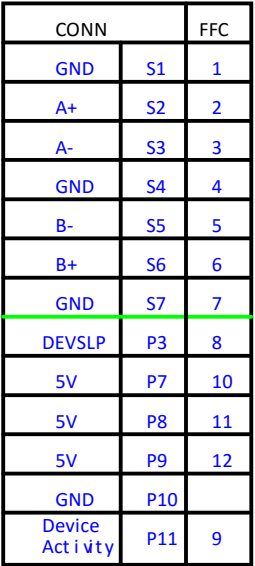
TEMPERATURE (°C)	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
7.7	87	97	107	117	127
7.9KΩ	79	89	99	109	119
10.5KΩ	81	91	101	111	121
14KΩ	83	93	103	113	123
18.7KΩ	85	95	105	115	125

## Main Func = RTC

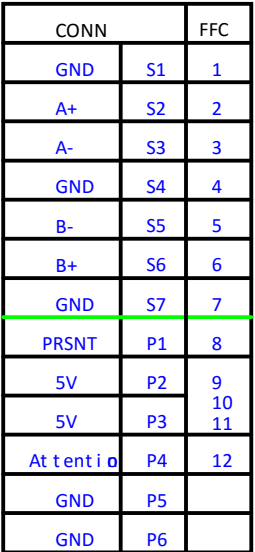


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## Main Func = HDD&FFS

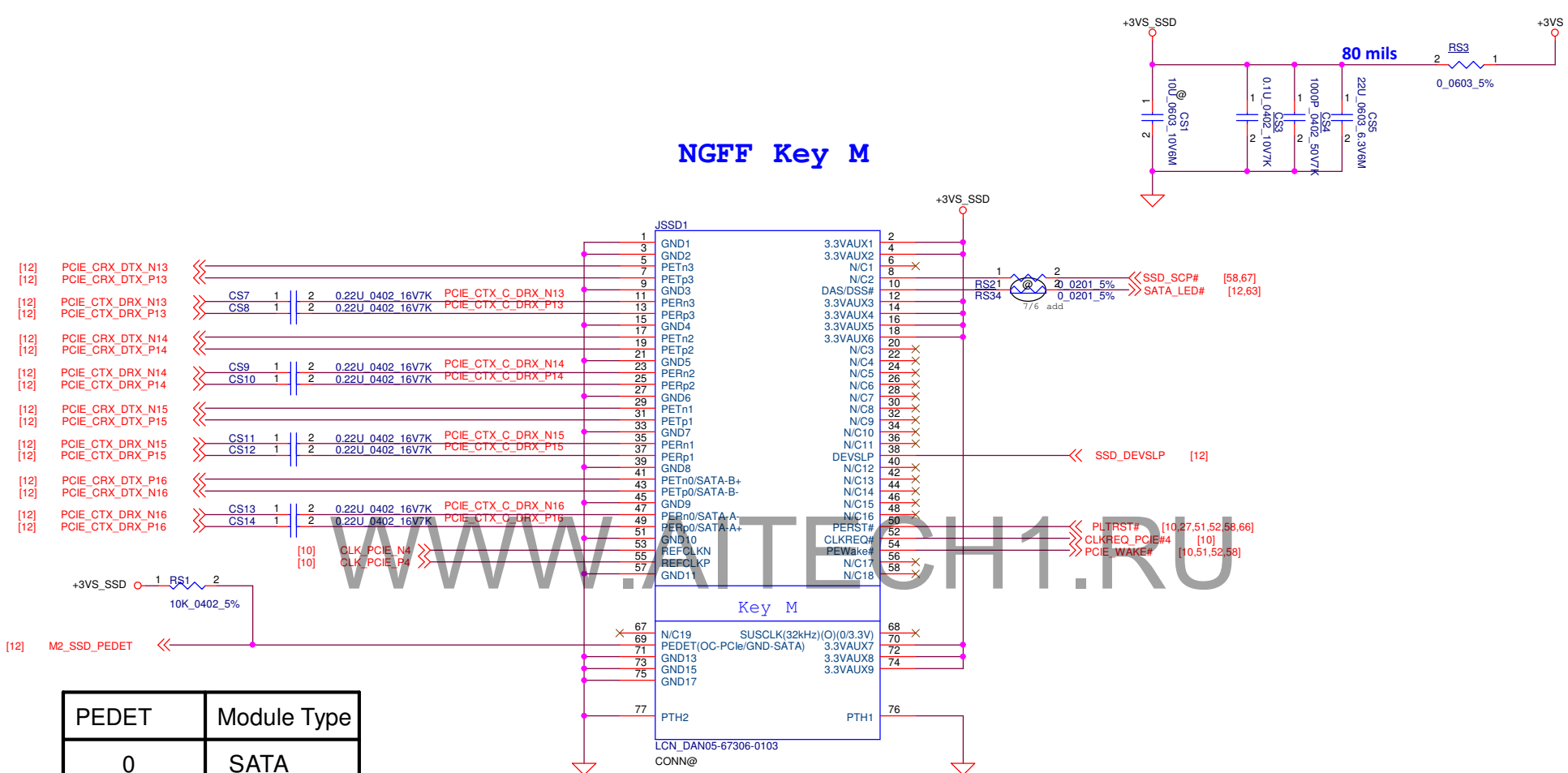


## Main Func = ODD

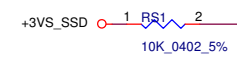


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				Size    Document Number    Rev Custom <b>LA-G716P</b> 1.0	
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NGFF Key M



- [12] PCIE\_CRX\_DTX\_N13
- [12] PCIE\_CRX\_DTX\_P13
- [12] PCIE\_CTX\_DRX\_N13
- [12] PCIE\_CTX\_DRX\_P13
- [12] PCIE\_CRX\_DTX\_N14
- [12] PCIE\_CRX\_DTX\_P14
- [12] PCIE\_CTX\_DRX\_N14
- [12] PCIE\_CTX\_DRX\_P14
- [12] PCIE\_CRX\_DTX\_N15
- [12] PCIE\_CRX\_DTX\_P15
- [12] PCIE\_CTX\_DRX\_N15
- [12] PCIE\_CTX\_DRX\_P15
- [12] PCIE\_CRX\_DTX\_P16
- [12] PCIE\_CRX\_DTX\_N16
- [12] PCIE\_CTX\_DRX\_N16
- [12] PCIE\_CTX\_DRX\_P16



[12] M2\_SSD\_PEDET

PEDET	Module Type
0	SATA
1	PCIE



Main Func = eMMC

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				Size	Document Number	Rev
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Date: Thursday, June 20, 2019				Sheet	69 of 101	

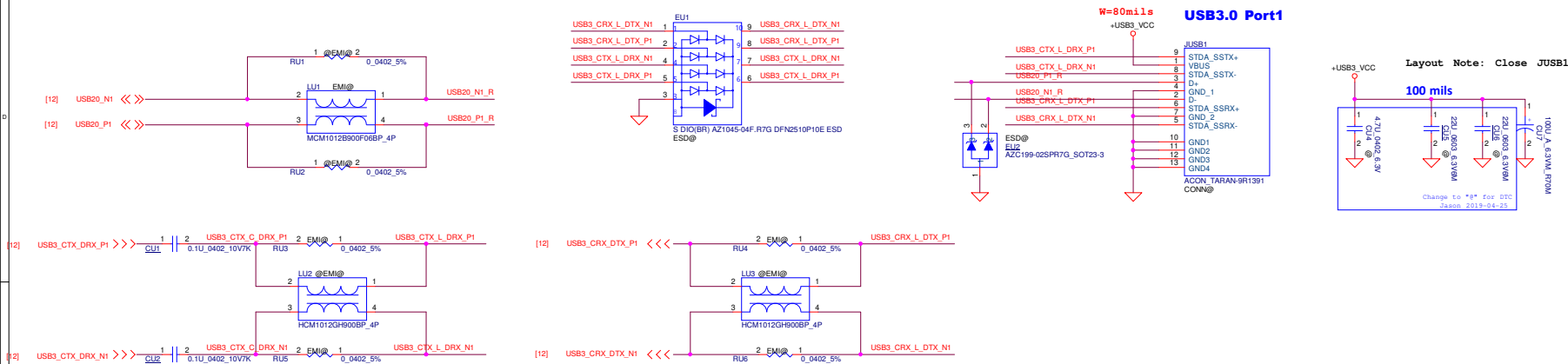
Main Function:

Reserve

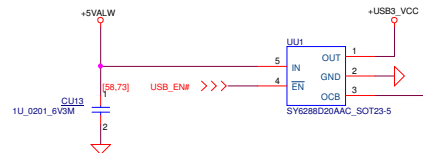
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# Main Func = USB3.0 Port1

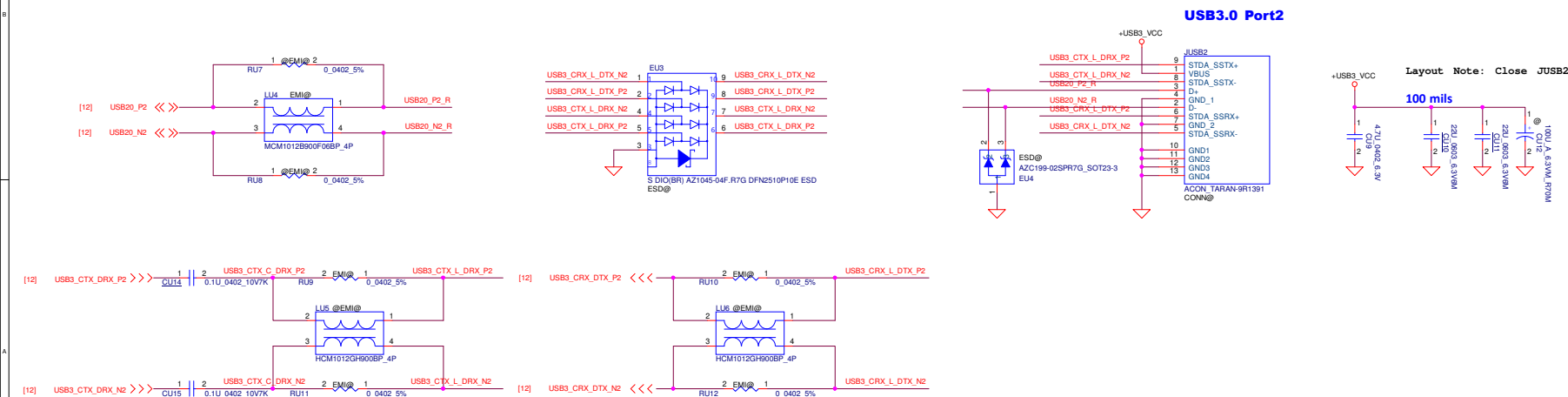


Maximum Output Current 2A



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# Main Func = USB3.0 Port2



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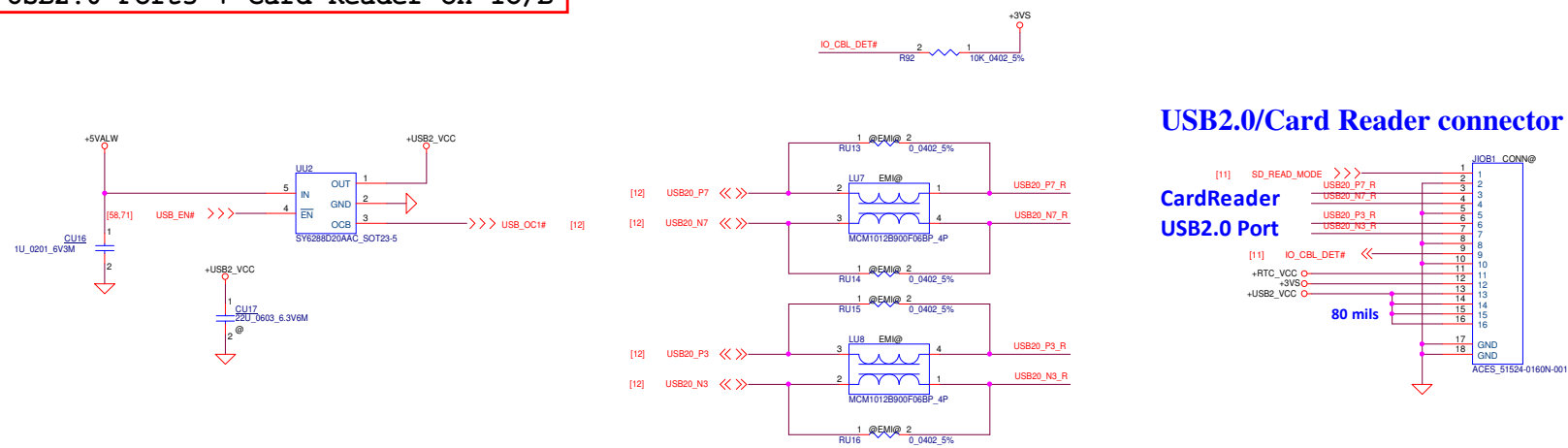
Main Function:

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Main Func = USB2.0 Port3 + Card Reader on IO/B



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Main Function:

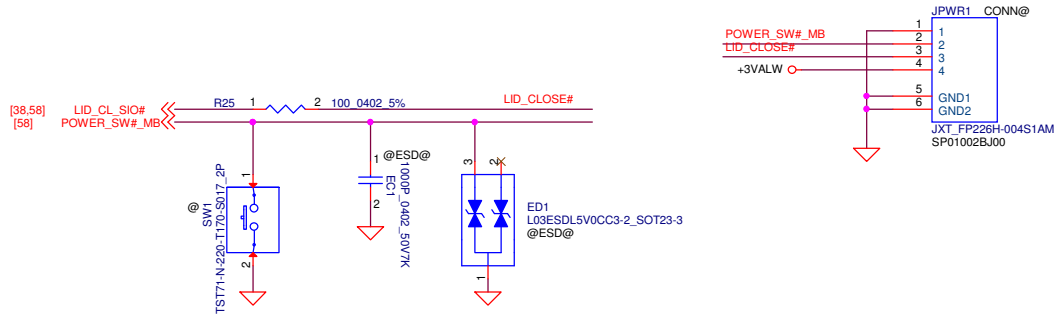
Reserve  
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Main Func = Power BTN

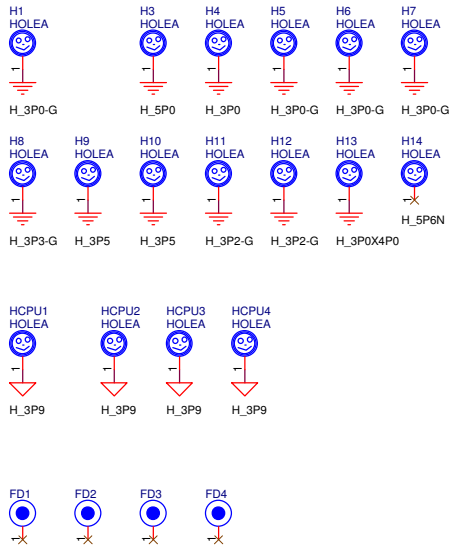
Low actived from KBC GPIO



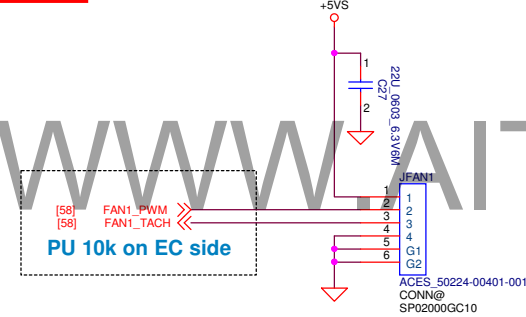
For EMI Reserved



Screw hole/FD

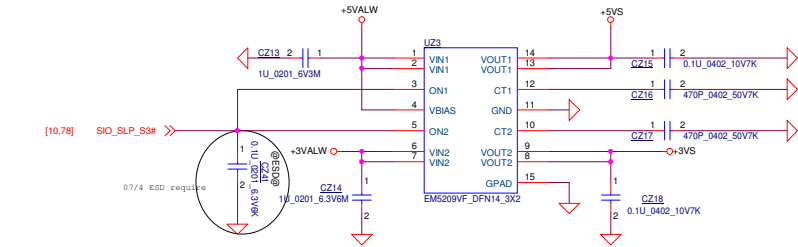


FAN

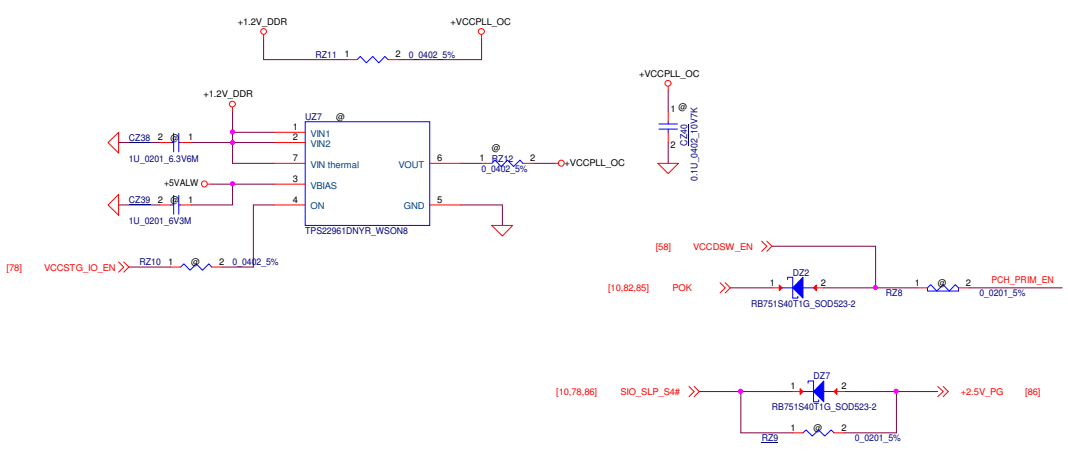


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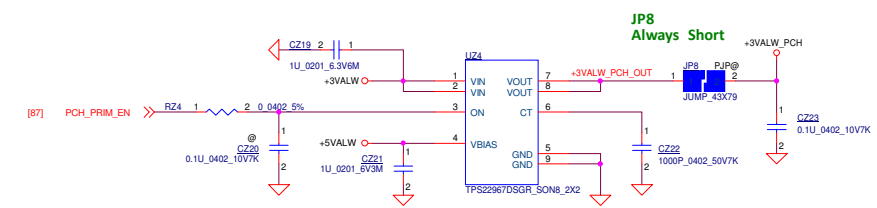
+5VS/+3VS for System



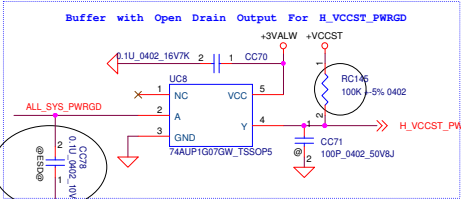
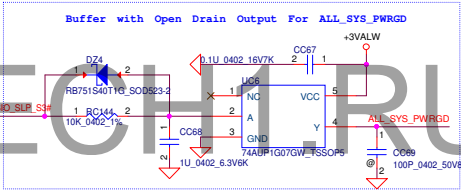
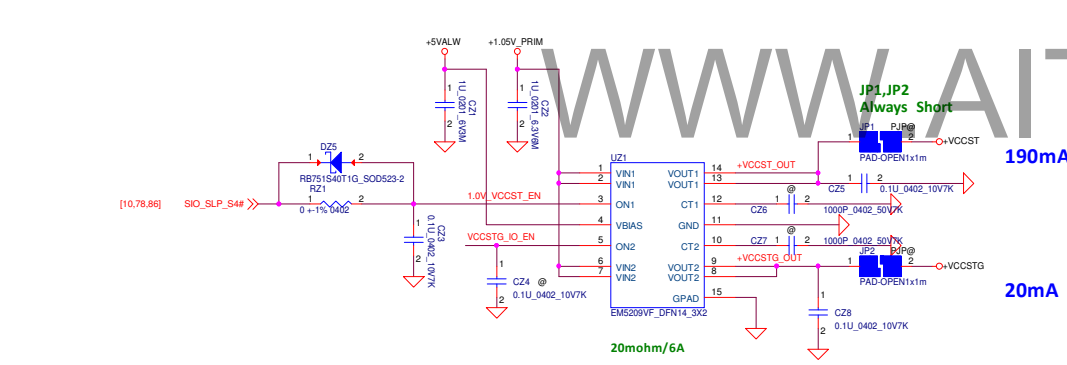
+VCCPLL\_OC source



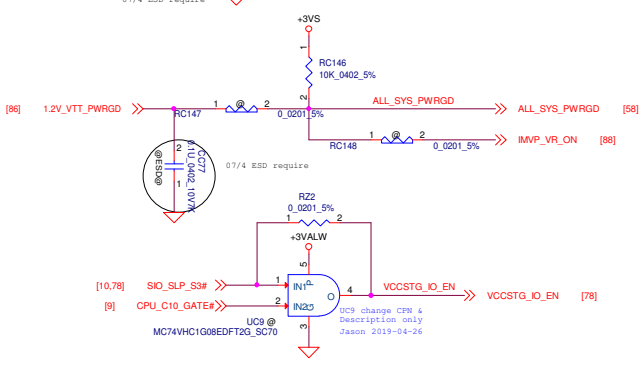
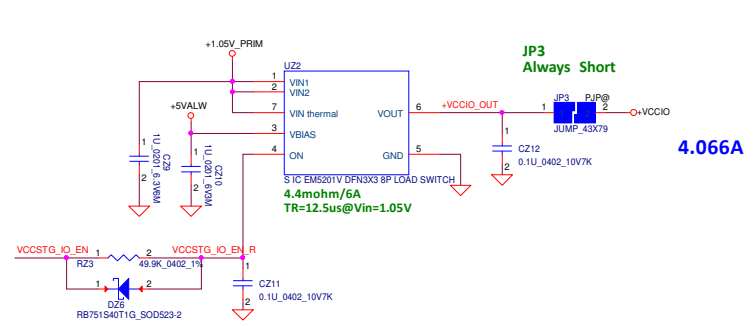
+3VALW\_PCH for System



+1.05V\_PRIM TO +VCCST /+VCCSTG



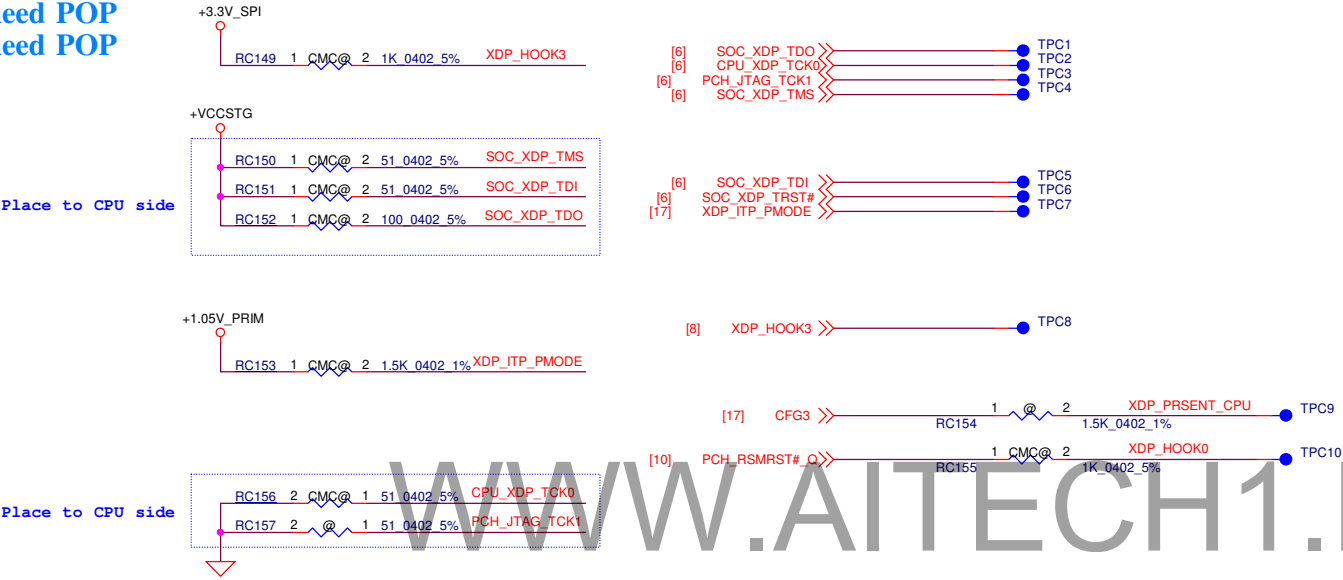
+1.05V\_PRIM TO +VCCIO





PortConnector Less Routing Topology


Follow KBL DCI Link  
RC152 need POP  
RC156 need POP



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**SPEC = 6KV**

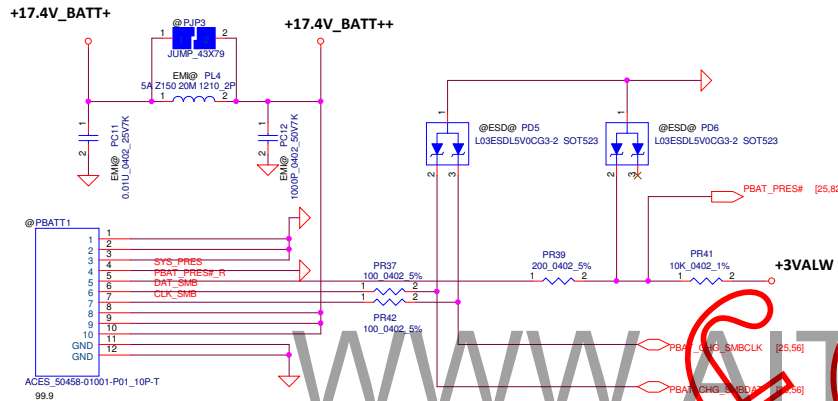
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Main Func = BATT CONN

Bat tery Bat Side

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Bat t+  
PIN9 Bat t+  
PIN10 Bat t+  
SP021412220

ACES\_50458-01001-P01\_10P-T



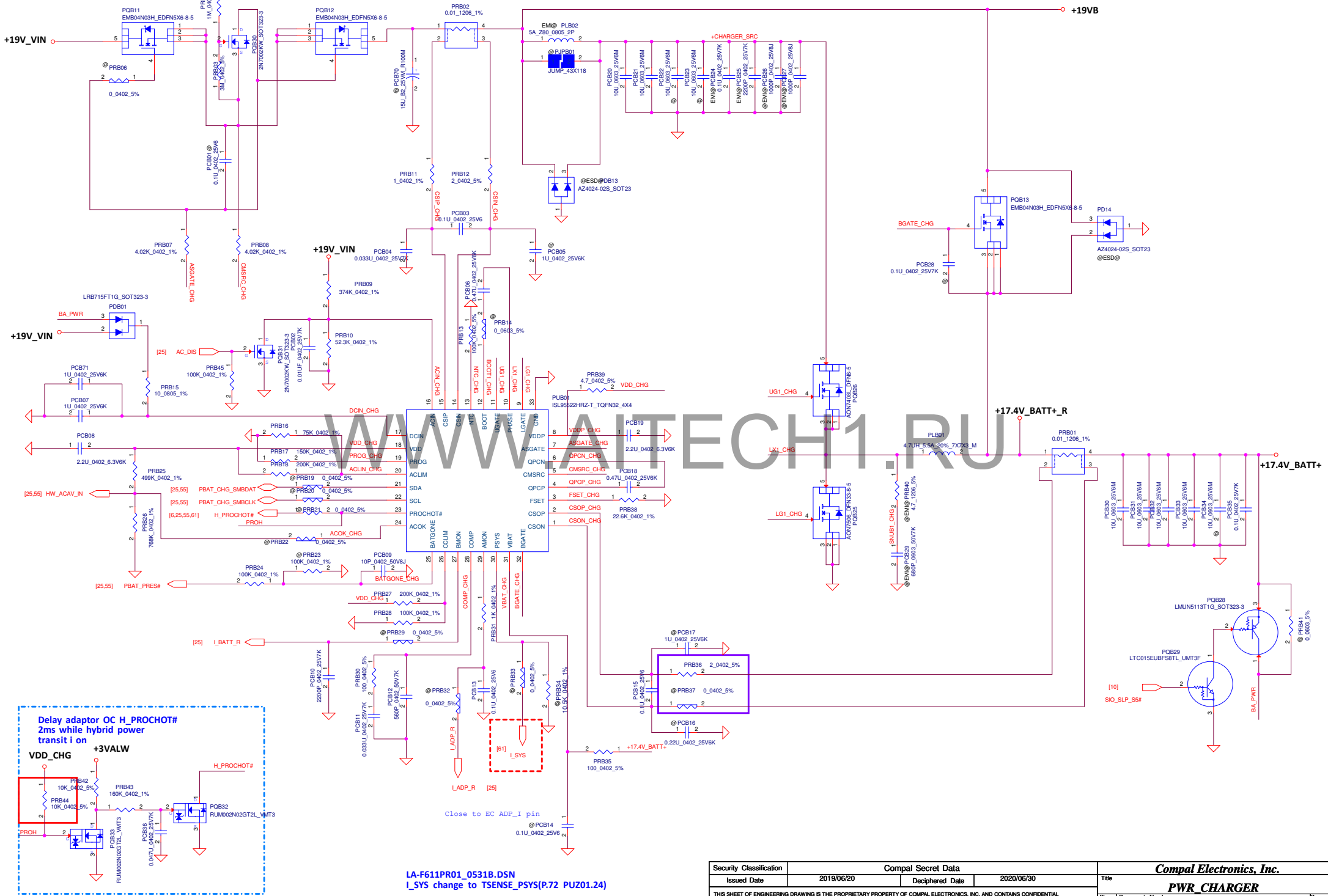
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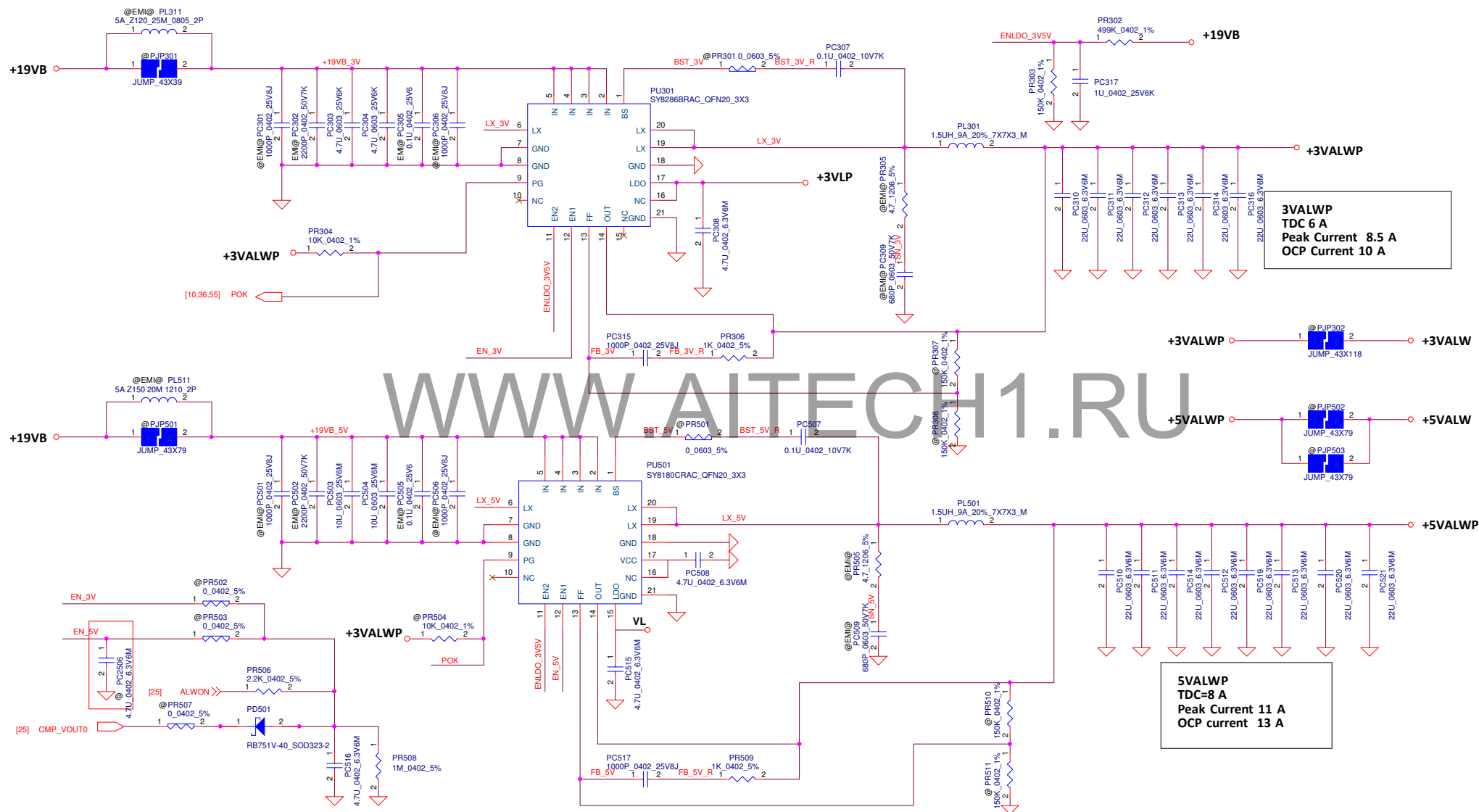
**Main Func = CHARGER**



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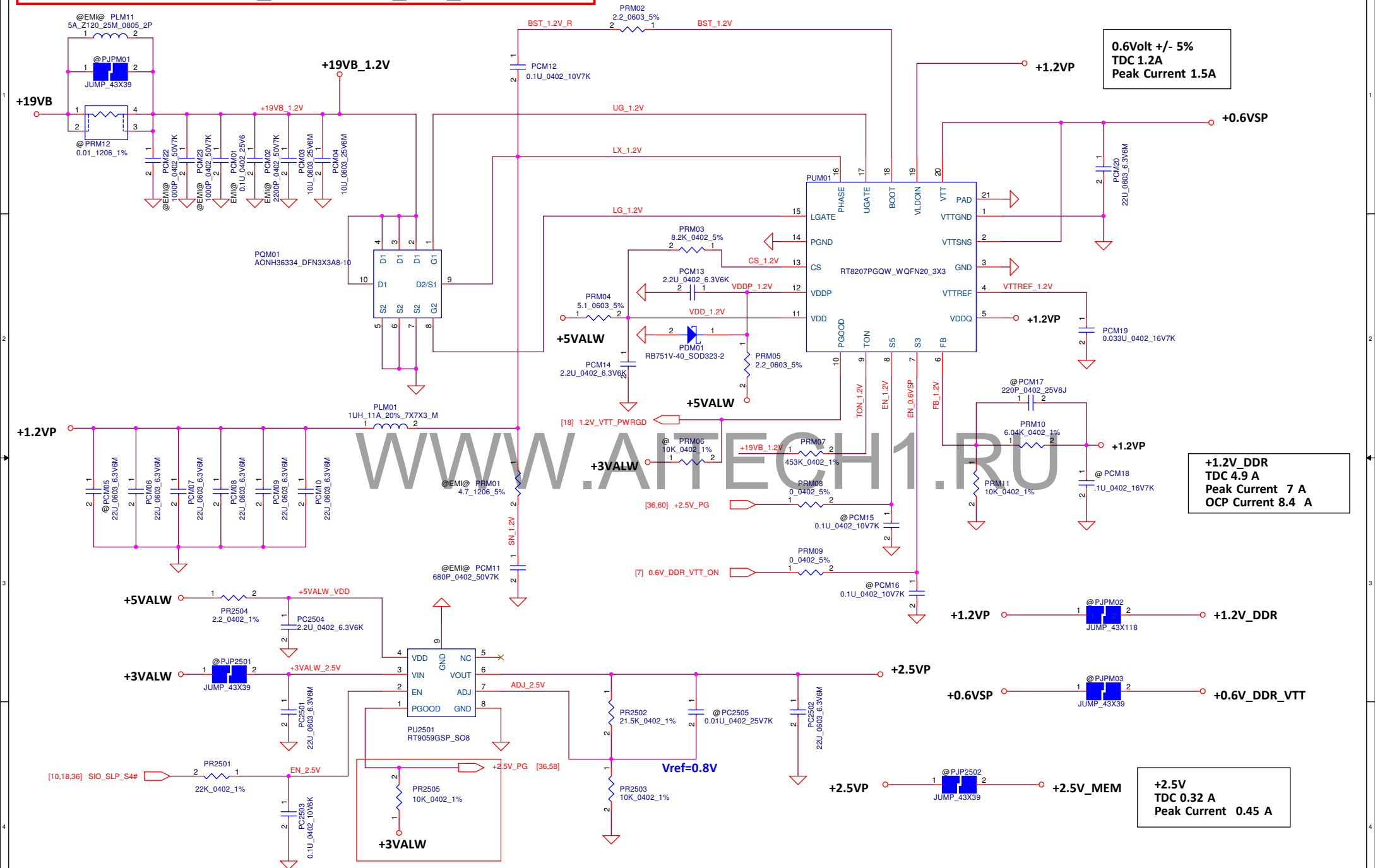


**Main Func = 3.3VALWP/5VALWP**



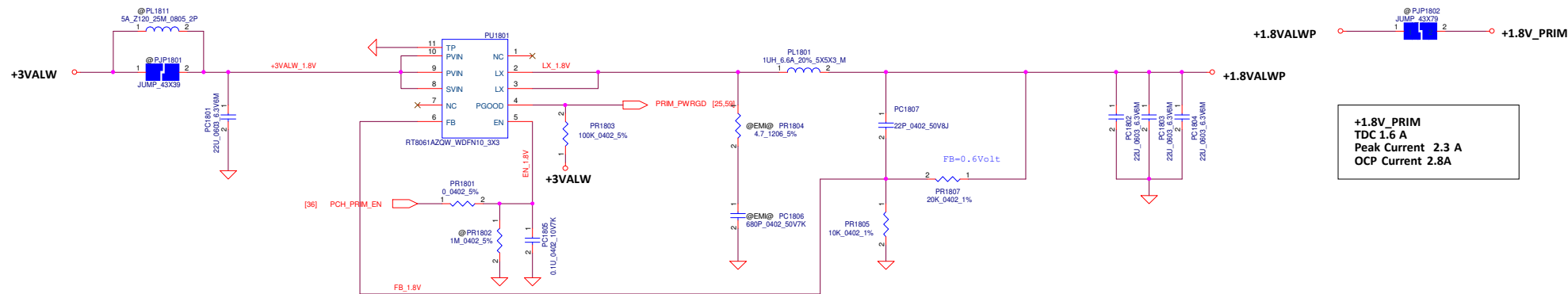
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**Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT/+2.5VP**



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**Main Func = +1.8VALWP /+1.05VALWP**



**+1.8V\_PRIM**  
**TDC 1.6 A**  
**Peak Current 2.3 A**  
**OCP Current 2.8A**

+1.05VALWP  
TDC 6.7 A  
Peak Current 9.5 A  
OCP Current 12 A Fix by IC  
Choke DCR 11.0mohm , 12.0mohm

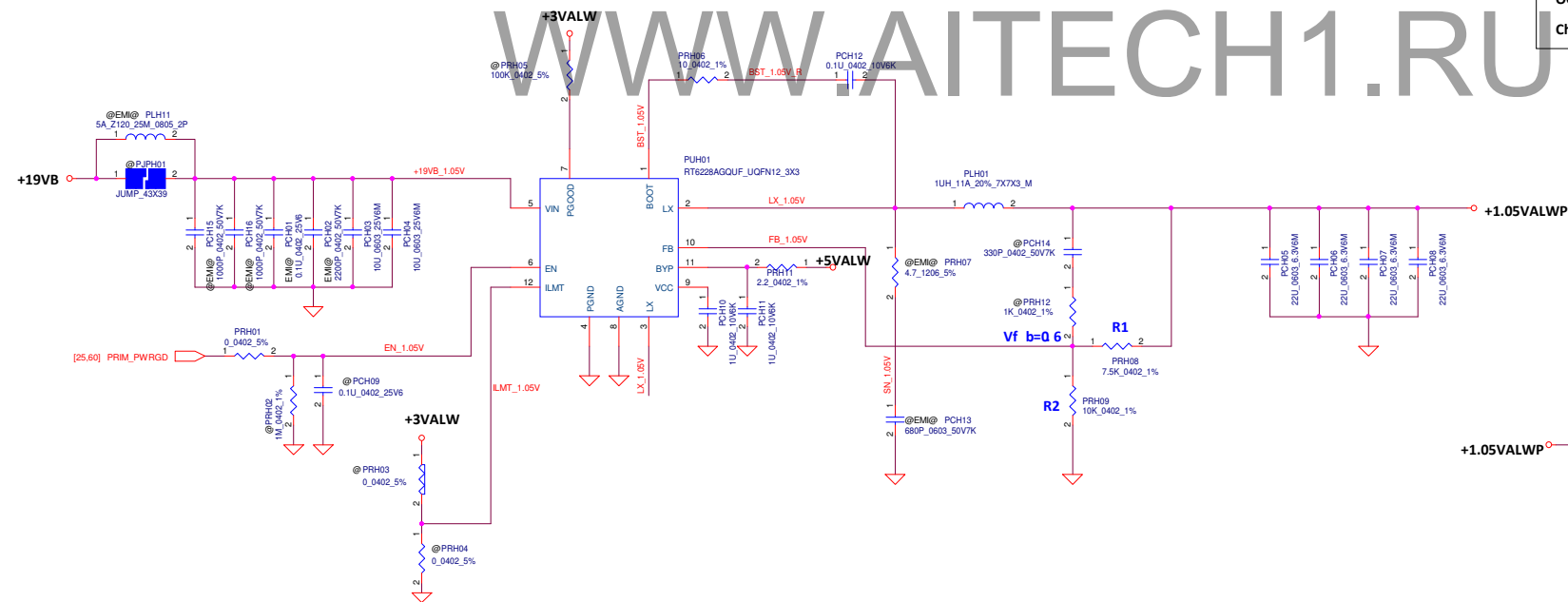
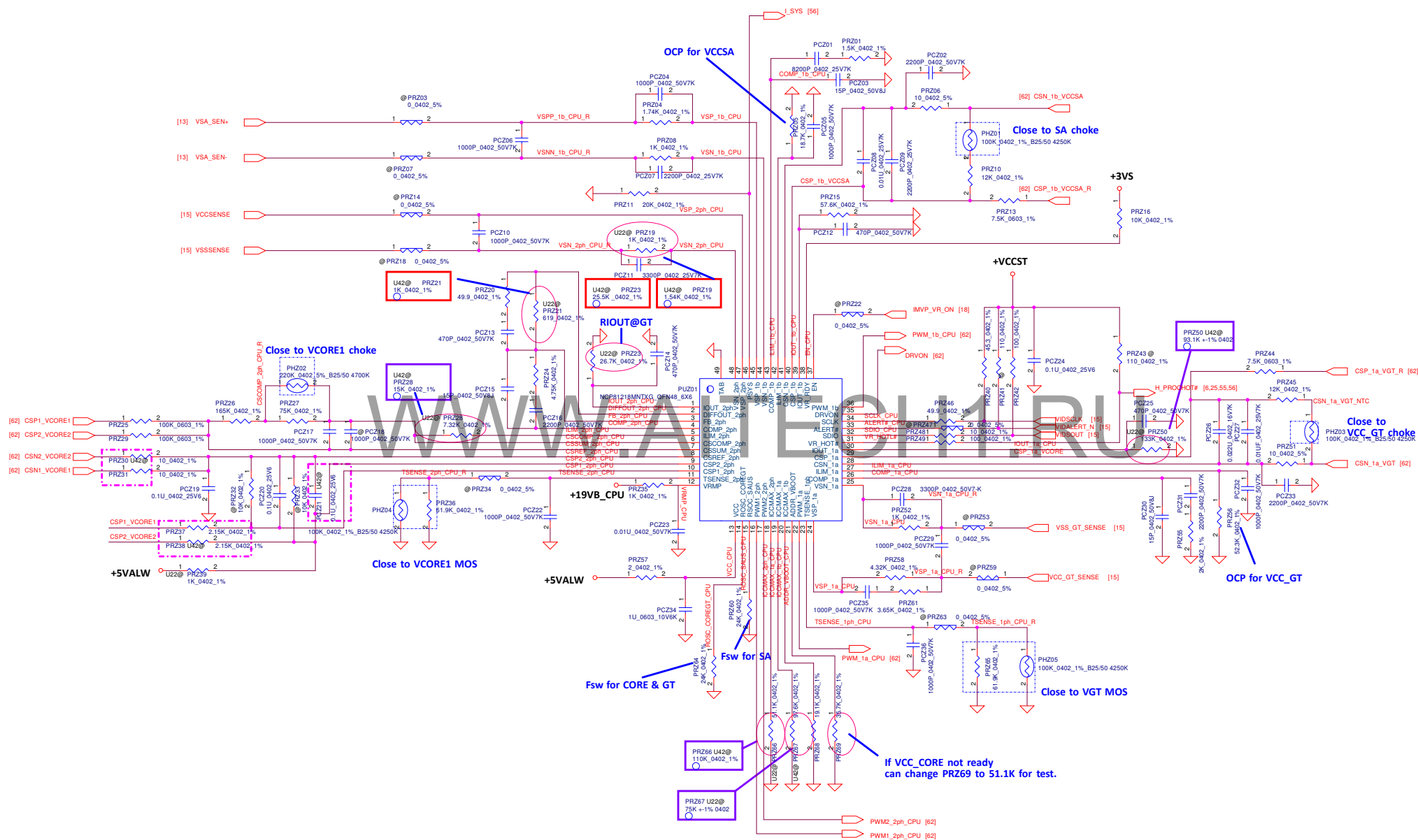


Diagram illustrating the connection between the **+1.05V<sub>ALWP</sub>** and **+1.05V<sub>PRIM</sub>** pins. The connection is made via a **JUMP 43X118** component, which is represented by a blue box with two terminals labeled **1** and **2**.

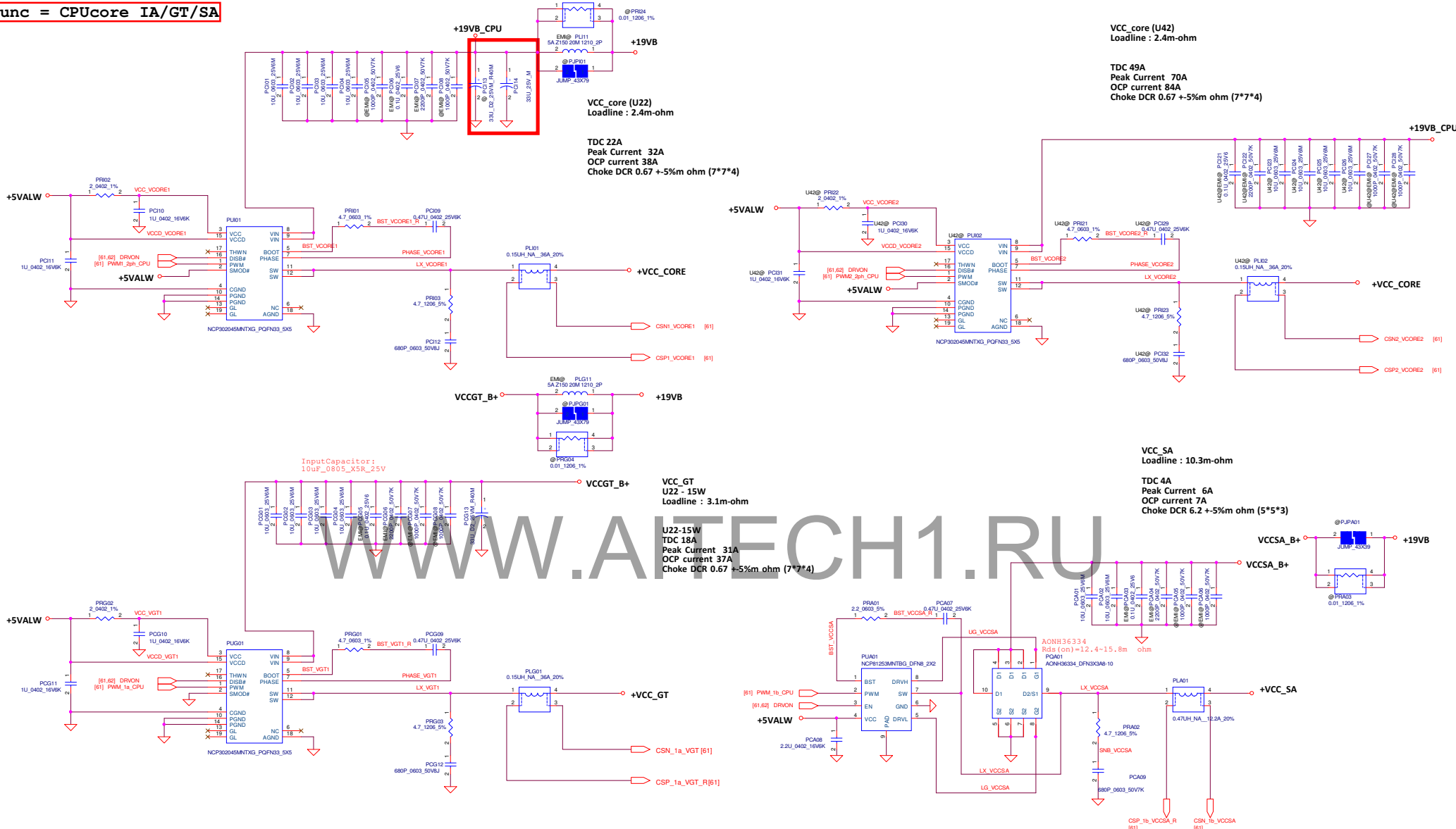
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**Main Func = CPU**



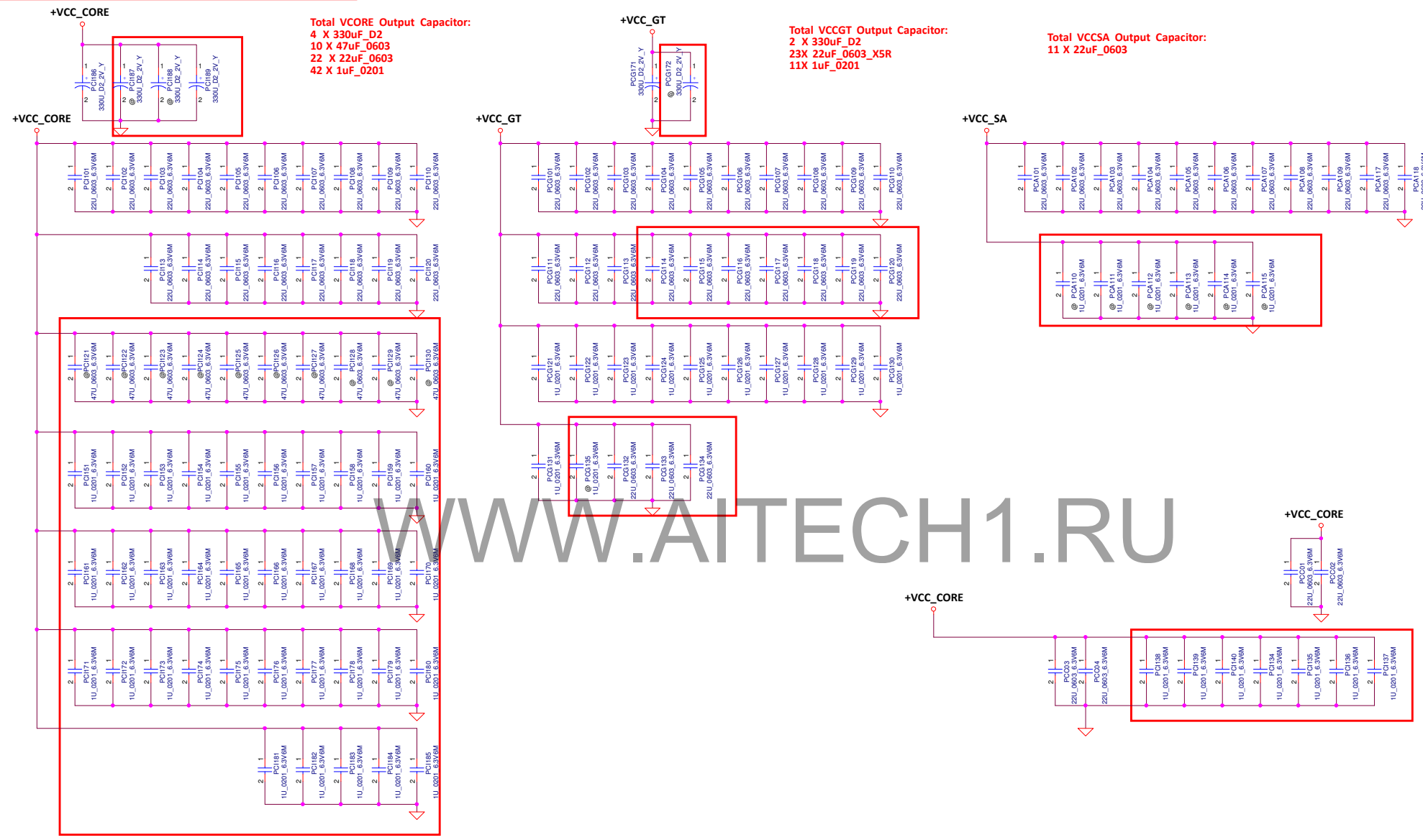
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Main Func = CPUcore IA/GT/SA




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Main Func = CPU / VGA / SA MLCC



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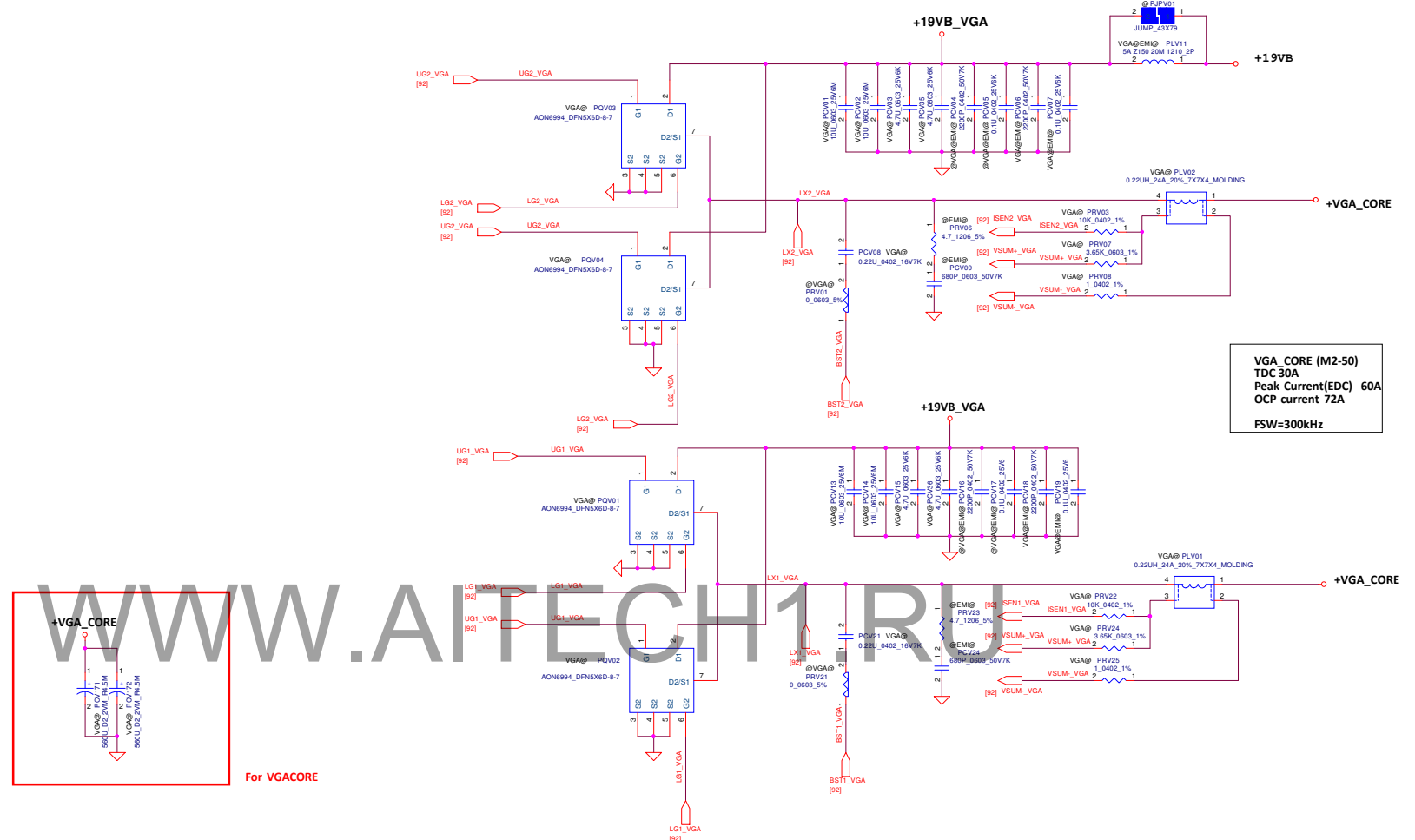
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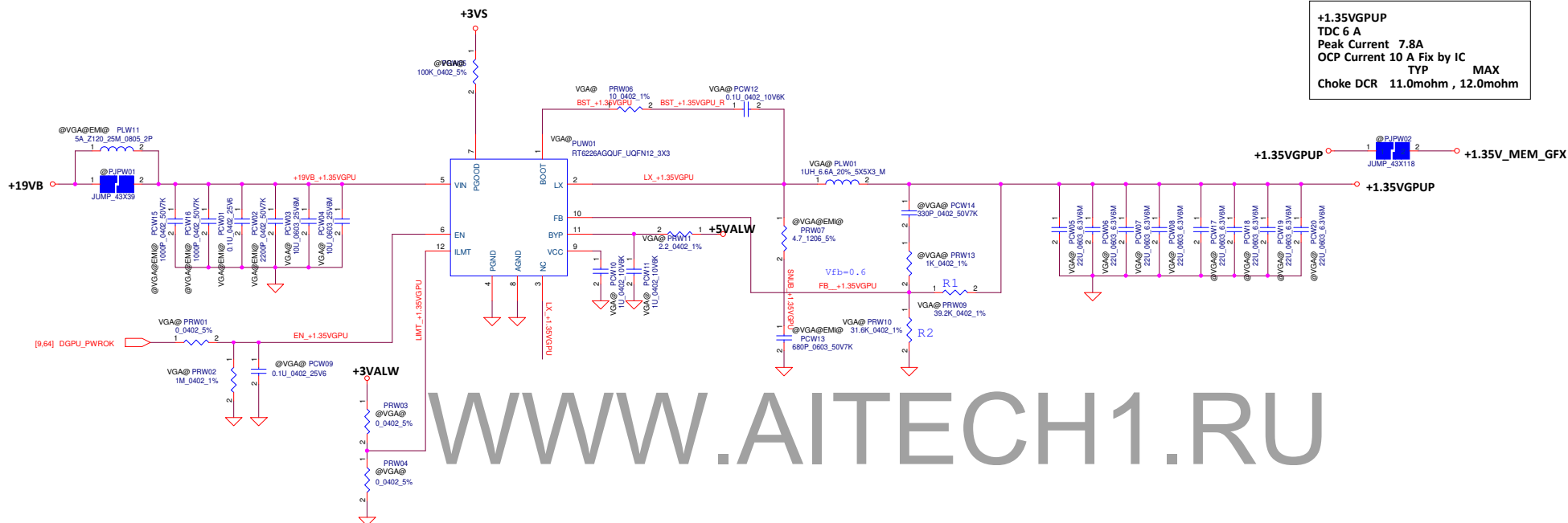




Main Func = VGA CORE



Main Func = +1.35VG PUP




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Version Change List ( P. I. R. List )

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PRB11 from 20hm to 10hm	X01
2.	P84-PWR_CHARGER	2018 06/12	Compal	Downsize	Change the PCB06 and PCB18 to 0.47U_0402	X01
3.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PCB11 to 0.33U	X01
4.	P89-PWR_CPU_Stage	2018 06/14	Compal	Downsize	PCA07, PCG09, PCI09, PCI29 change to 0.47U_0402	X01
5.	P92-PWR_VGA_CORE(ISL62771)	2018 06/14	Compal	Downsize	Change PCV30 to 0.15U_0402 Change PCV32 to 0.1U_0402	X01
6.	P86-PWR_1.2V_DDR	2018 07/05	Compal	Factory suggest	Change the PDM01 to SCS00000Z00	X01
7.	P83-BATT_CONN	2018 07/05	Compal	ESD request	Change the PD5,PD6 to SCA00002A00	X01
8.	P84-PWR_CHARGER	2018 07/09	Compal	Modify for AC detect	Change the PRB10 from 47K to 52.3K	X01
9.	P90-PWR_CPU MLCC	2018 07/09	Compal	Change for PI simulat i on	move PCI134,PCI135,PCI136,PCI137,PCI138, PCI139,PCI140 to +VCC_CORE_GT	X01
10.	P84-PWR_CHARGER	2018 07/11	Compal	Factory request	Add PCB71, PCB07 change to 1U_0402	X01
11.	P92-PWR_VGA_CORE	2018 07/17	Compal	Downsize	Change the PCV30 to SE000011G00 0.15U 16V	X01
12.	P88-PWR_CPU	2018 07/17	Compal	Change for CPU EA test	Change the PRZ25, PRZ29 to SD014100380 100K Change the PRZ23 to SD034255200 25.5K	X01

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